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Systematic Investigation of Metal Gates on Atomic-Layer-Deposited HfO_2

Hyundoek Yang and Hyunsang Hwang*

Department of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju 500-712, Korea

For *n*-type metal-oxide-semiconductor devices with HfO_2, a metal gate with a very low workfunction is necessary. However, the Fermi level pinning effect shifts an effective workfunction $\Phi_{m,eff}$ of the metal on HfO_2 towards a midgap value. In this paper, we systematically evaluate the $\Phi_{m,eff}$ values of various metal gates on atomic-layer-deposited HfO_2 with and without surface treatments. Using high-pressure wet post-deposition-annealing (1-step process) or a wet-solution treatment after conventional post-deposition-annealing (2-step process), we could dramatically reduce the extrinsic pinning. The effective workfunction of ScN_x gates on the surface-treated HfO_2 was ~4 eV, similar to that of the ScN_x/SiO_2 samples. Therefore, ScN_x metal gate is a good candidate for atomic-layer-deposited HfO_2.

Keywords: metal gate, high-k, dielectric, MOS, pinning, workfunction, ScN, high pressure

1. INTRODUCTION

The scaling of equivalent oxide thickness (EOT) is the most important issue in the development of metal-oxide-semiconductor field effect transistor (MOSFET) devices. Compared with SiO_2, transition metal oxides with high dielectric constants (high-*k*) have an enormous advantage in EOT scaling with lower leakage current[1]. HfO_2 is a representative candidate for the next generation MOSFET devices, due to its high dielectric constant and excellent thermodynamic stability[2]. The metal gates, especially with low workfunction values for *n*-type MOS (NMOS) devices, are another important issue. Metal gates have been introduced to replace the conventional poly-Si gate which shows high sheet resistance, boron penetration, and Fermi level pinning (FLP), as well as an increase of EOT due to gate depletion[3]. The FLP effect of metal gates is not clearly understood yet, particularly with respect to whether the effect depends on dielectrics[4-8]. The suggested FLP consists of intrinsic FLP and extrinsic FLP. The intrinsic FLP is originated by the generation of charged dipole near at intrinsic interface states on high-k gate dielectrics[4]. The extrinsic FLP is generated by the extrinsic surface states related to chemical bonding and oxygen vacancies[9-15]. The chemical bonding between Si atoms in poly-Si or fully-sillicide (FUSI) gate and Hf atoms in HfO_2 results in a shift of the effective workfunction ($\Phi_{m,eff}$) toward a midgap value[9-11]. The oxygen vacancies caused by oxygen transport across the metal/dielectric interface are also an important factor of the extrinsic FLP[13-15].

For NMOS or dual metal gates, various materials have been evaluated. Compared with nitride and silicide metal gates, pure metal gates offer low resistivity. However, NMOS-compatible pure metals have very low electronegativity values and result in reactions with dielectrics. The Hf gate on SiO_2 reduces the underlying SiO_2 and generates high-k dielectrics near the gate/dielectric interface[16]. The Ti gate on the HfO_2/SiO_2 stack reduces the interfacial SiO_2 layer without any interaction between Ti and HfO_2[17]. Metal alloys such as Ru-Ta, Pt-Ta, and Ni-Ti have been suggested for dual-metal gates by using a *p*-type-MOS (PMOS)-compatible metal and an NMOS-compatible metal[18-20]. However, the alloys may have limited use due to the reactive NMOS-compatible pure metal. To overcome the poor thermal stability and the difficulty of controlling the EOT when using reactive pure metals, various metal compounds have been evaluated. It has been reported that a ZrN gate on HfSiON has an NMOS-compatible $\Phi_{m,eff}$ of ~4.25 eV[21]. However, most binary metal nitrides including TaN_x, TiN_x, and HfN_x are not appropriate for NMOS devices[22-24]. It has been reported that the $TaSi_xN_y$ gate is a promising NMOS-compatible candidate with a $\Phi_{m,eff}$ value of about 4.3~4.6 eV[6,25,26]. The lanthanide-incorporated metal nitrides on SiO_2 have NMOS-compatible $\Phi_{m,eff}$ values[27]. In addition to nitrides, both boride and carbide can be NMOS candidates. LaB_6 is an NMOS-compatible gate on SiO_2, but shows significant extrinsic FLP for devices with HfO_2[5]. A TaC_x gate on HfO_2 having an NMOS-compatible $\Phi_{m,eff}$ value of

*Corresponding author: hwanghs@gist.ac.kr

~ 4.18 eV has also been reported[5].

In this paper, we systematically evaluate the $\Phi_{m,eff}$ values of various metal gates on atomic-layer-deposited (ALD) HfO_2 with and without surface treatment. Oxygen passivation of the HfO_2 surface by high-pressure wet post-deposition-annealing (HP-wet-PDA) and wet-solution treatments dramatically reduces the extrinsic FLP for metal with a very low workfunction value.

2. EXPERIMENTS

Using the ALD process, we deposited HfO_2 films with different thicknesses on 8-inch Si wafers with ultrathin SiO_2 interfacial layers. We evaluated various metal gates and surface treatments of HfO_2, as summarized in Table 1. Binary metal nitrides (TaN_x, HfN_x, TiN_x, and ScN_x) were deposited by reactive sputtering with various N_2 gas flow rates. To evaluate the effect of impurities such as B, C, and N, we used Ta-based sputter targets (TaB_2, TaC, and TaN). In addition, TaC_x gates were deposited by reactive sputtering with various CH_4/Ar gas flow rates. Lanthanide-incorporated metal nitrides were deposited by co-sputtering of the TaN target with lanthanide elements (Dy, Gd, Sm, and Tb). In order to prevent oxidation of the surface, all metal gates were capped with 200 nm-Pt without breaking the vacuum condition. The base pressure and working pressure of the used rf magnetron sputtering system were ~5×10^{-7} Torr and ~1×10^{-3} Torr, respectively. To reduce the oxygen vacancies on HfO_2, some samples were surface-treated before depositing the gates. The surface treatments comprised HP-wet-PDA and wet solutions such as tetramethyl ammonium hydroxide (TMAH), hydrogen peroxide (H_2O_2), and ammonium hydroxide (NH_4OH). The conventional PDA was performed in O_2 ambient at 450 °C for 30 min except for the HP-wet-PDA samples. For all the samples, post-metallization annealing in forming gas ambient (FG-PMA) was performed. The area of gates and the substrate concentration are 2.5×10^{-5}cm^2 and ~1×10^{15}cm^{-3}, respectively.

The physical thicknesses of HfO_2 (T_{HfO_2}) were determined by X-ray reflectivity (XRR). The electrical characteristics including capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) characteristics were evaluated using a HP 4284A Precision LCR Meter and a HP 4155A Semiconductor Parameter Analyzer. The EOT and flat-band voltage (V_{fb}) values of the MOS devices were extracted by the Berkeley simulator[28]. The $\Phi_{m,eff}$ values of the metals on the HfO_2/SiO_2 stack were extracted by considering both the interfacial SiO_2 thickness (T_{SiO2}) and the fixed charge[29].

3. RESULTS AND DISCUSSION

Fig. 1(a) shows a plot of the EOT versus T_{HfO2}. The T_{HfO2} values were determined by XRR, as shown in Fig. 1(b). The relation between EOT and T_{HfO2} is given by

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} T_{HfO_2} + T_{SiO_2} \quad (1)$$

where ε_{SiO_2} and ε_{HfO_2} are the dielectric constants of SiO_2 and HfO_2, respectively. Therefore, from the slope and the intercept of a linear fit to the plot of the EOT versus T_{HfO_2}, the ε_{HfO_2} and T_{SiO_2} values can be respectively extracted by Eq. (1). ε_{HfO_2} was ~18 and T_{SiO_2} was ~1 nm. The extracted ε_{HfO_2} value is nearly the same as the reported value of ALD-HfO_2[30].

Fig. 2 summarizes the reported $\Phi_{m,eff}$ versus the metal vacuum workfunction ($\Phi_{m,vac}$) relations. The FLP effect significantly increases the $\Phi_{m,eff}$ values of HfO_2 devices, especially for metals with very low $\Phi_{m,vac}$ values. The LaB_6 gates on SiO_2 and HfO_2 show significant extrinsic FLP[4-6]. Therefore, compared with SiO_2, new materials with lower $\Phi_{m,vac}$ values are necessary for NMOS devices with HfO_2. In addition, the suppression of extrinsic FLP is needed for an NMOS-compatible $\Phi_{m,eff}$ value.

Considering the $\Phi_{m,vac}$ value of Sc (~ 3.5 eV), the $\Phi_{m,eff}$ value of Sc on HfO_2 is expected to be appropriate for NMOS devices[4,31]. Fig. 3(a) shows the C-V characteristics of the MOS capacitors with Sc gates on ALD-HfO_2 after FG-PMA at various temperatures. The capacitance values in the strong

Table 1. Experiments to obtain the appropriate workfunction

Appropriate Workfunction → Materials / Surface Treatment

Materials

Pure Metal	Sc, Ta, Ti, Pt
Nitride	TaN, HfN, TiN, ScN TaDyN, TaGdN, TaSmN, TaTbN
Carbide	TaC
Boride	TaB_2

Surface Treatment

Wet Solution	TMAH (25 %) : 70 °C 5 min H_2O_2 (10 %) : 35 °C 20 min NH_4OH (20 %) : 35 °C 30 min
HP-Wet-PDA	5~10atm, 200~300 °C, 20 min

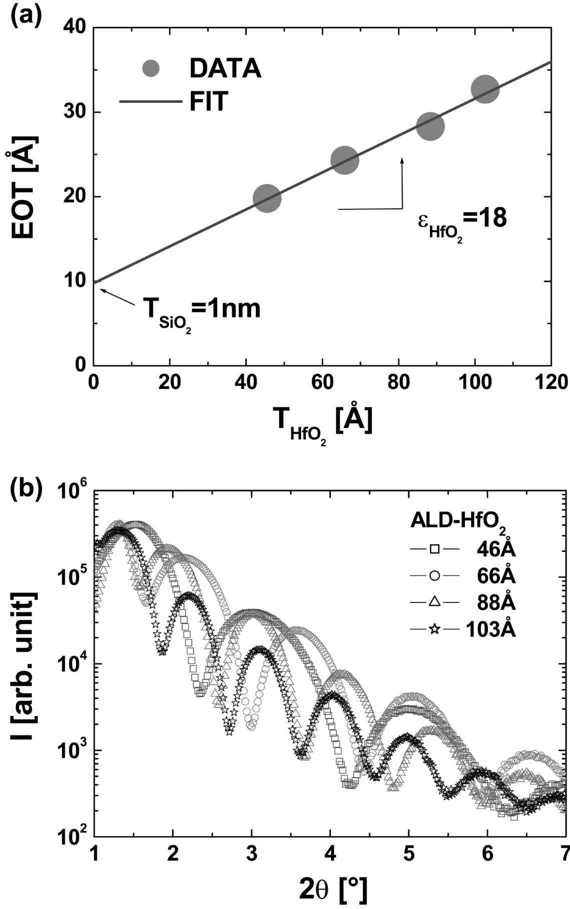

Fig. 1. (a) EOT versus T_{HfO2} plot. From the slope and the intercept, ε_{HfO_2} and T_{SiO_2} respectively can be determined. (b) XRR data of the prepared ALD-HfO_2 after O_2-PDA at 450 °C for 30 min.

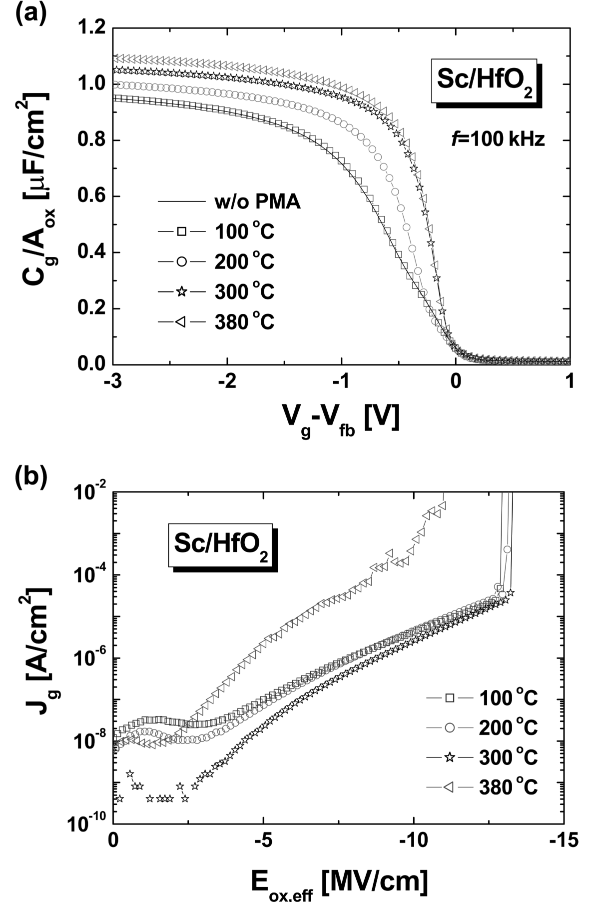

Fig. 3. (a) C-V and (b) I-V characteristics of Sc/HfO_2 with various FG-PMA temperatures. EOT decreases above 200 °C due to the reactive Sc gate. The leakage current increases above 300 °C.

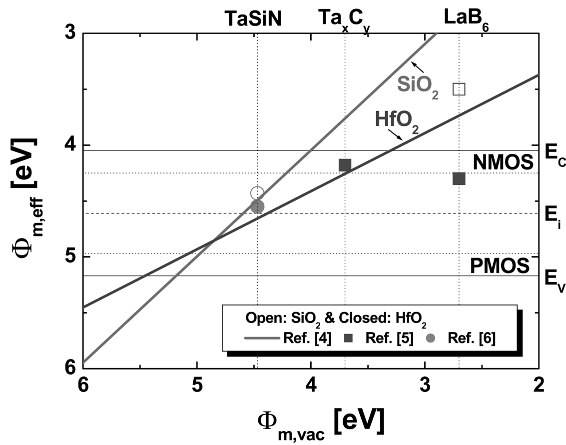

Fig. 2. Summary of the reported $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ relations. A metal gate with a low $\Phi_{m,vac}$ value (less than ~4 eV) is needed for an NMOS with HfO_2. The LaB_6 shows significant extrinsic FLP.

accumulation regime reveal that the EOT decreases as the FG-PMA temperature increases, even at 200 °C. The reduction of the EOT can be explained by the oxygen-gettering effect of Sc[17]. The high oxygen solubility of Sc results in oxygen diffusion from the interfacial SiO_2 layer to the gate electrode. Fig. 3(b) shows the I-V characteristics of the Sc samples. Up to 300 °C, the leakage current density (J_g) in the high electric field (E_{ox}=(V_g-V_{fb})/EOT) regime is nearly unchanged, even though the EOT is decreased. This result suggests that for these annealing conditions the Sc gate has no effect on the quality of the HfO_2 film. However, the FG-PMA at 380 °C significantly increases the leakage current. This increase means that the quality of HfO_2 is degraded at 380 °C by the interface reaction[32]. A Ti gate can also be used for an oxygen-gettering electrode[17]. However, higher temperature is required for the EOT scaling by the Ti gate. As shown in Fig. 4, the Ti gate sample annealed at 440 °C and the Sc gate sample annealed at 300 °C show a comparable reduction in the EOT (ΔEOT=3Å). Although both samples show the same EOT, the leakage current of the Ti sample is significantly higher than that of the Sc sample, as shown in the inset figure of Fig. 4. As with the Sc gate, the Ti

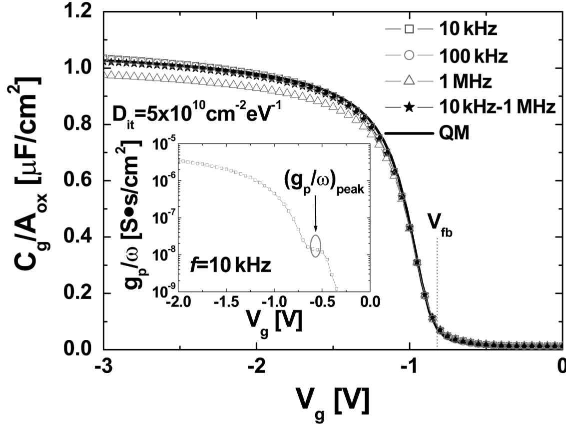

Fig. 4. C-V and G-V characteristics of Sc/HfO_2 after FG-PMA at 300 °C. The sample shows the excellent interfacial quality.

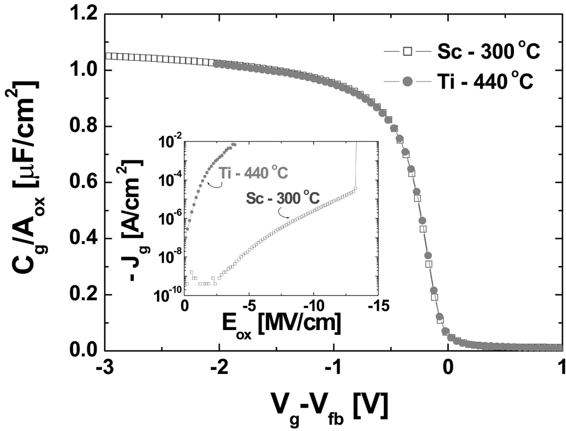

Fig. 5. Electrical characteristics of Sc and Ti gates on HfO_2. Compared with Ti, the Sc gate reduces EOT without increasing the leakage current.

gate increases the values of J_g at a relatively high temperature. Therefore, the Sc gate more efficiently decreases the EOT while maintaining low leakage current. Fig. 5 shows the C-V characteristics of the Sc sample after FG-PMA at 300 °C, measured at various frequencies (f=ω/2π). It can be seen that the frequency dispersion is negligible in the overall bias range. The slightly lower capacitance values at 1 MHz in the strong accumulation regime can be explained by the series resistance of the substrate and the gate[33]. Using the measurement at two frequencies and the three-element equivalent circuit model, a frequency-independent C-V curve can be obtained[33]. The corrected capacitances ($C_{10kHz\text{-}1MHz}$) from the data measured at 10 kHz and 1 MHz were in excellent agreement with the measured capacitances at 10 kHz and 100 kHz, as shown in Fig. 5. In addition to the negligible frequency dispersion, the measured curves were in good agreement with the curve calculated by the quantum-mechanical (QM) simulation[28]. This result means that the

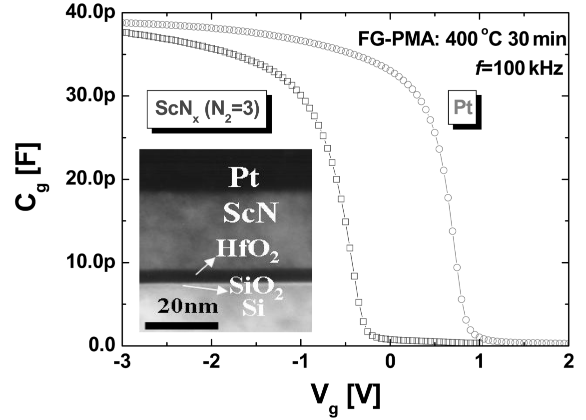

Fig. 6. C-V characteristics of Pt and ScN_x (N_2=3sccm) gates on 46 Å-HfO_2. Inset figure shows a TEM image of the ScN_x sample. The C-V and TEM results suggest that negligible interaction occurs at the ScN_x/HfO_2 interface.

Sc sample has good interfacial quality. In order to evaluate the interface trap density (D_{it}), the G-V characteristics were used, as shown in the inset of Fig. 5. In general, D_{it} is proportional to the value of the G_p/ω peak and the extracted value is about 5×10^{-10} $cm^{-2}eV^{-1}$. As a result, the excellent interfacial quality of the Sc sample can be retained even though the EOT is aggressively reduced. Considering the interfacial layer of the as-deposited sample and the ΔEOT value of the annealed sample, the excellent value of D_{it} may be due to the remaining interfacial SiO_2 layer near the Si substrate.

In order to overcome the poor thermal stability and the difficulty of controlling the EOT of the reactive pure metal with a very low workfunction, various reactive-sputtered metal nitrides were evaluated. Fig. 6 shows the stability of ScN_x at an N_2 flow rate of 3 sccm. The FG-PMA at 400 °C for 30 min was performed after depositing ScN_x and Pt gates on 46 Å-HfO_2/SiO_2 stacks. The strong accumulation regime reveals that the capacitance values of the ScN_x and Pt devices are nearly the same. The highly similar EOT indicates that a negligible reaction occurs near the interface between ScN_x and HfO_2. Examination of a TEM image of the ScN_x sample, shown in the inset of Fig. 6, confirms the negligible reaction at the ScN_x/HfO_2 interface. Fig. 7 shows the V_{fb}-EOT relations of the ScN_x gates on SiO_2 and HfO_2 with various N_2 flow rates. In the case of the SiO_2 samples, the V_{fb} versus EOT relation is given by

$$V_{fb} = \Phi_{m,eff} - \Phi_s - \frac{Q_{fixed}}{\varepsilon_{SiO_2}} EOT \qquad (2)$$

where Φ_s and Q_{fixed} are the workfunction of the substrate and the fixed charge in the SiO_2, respectively. From Eq. (2), V_{fb} is linearly dependent on the EOT. In Fig. 7, the ScN_x/SiO_2 samples show that the linear V_{fb}-EOT relations have nearly the same slope irrespective of the N_2 flow rate. In contrast to

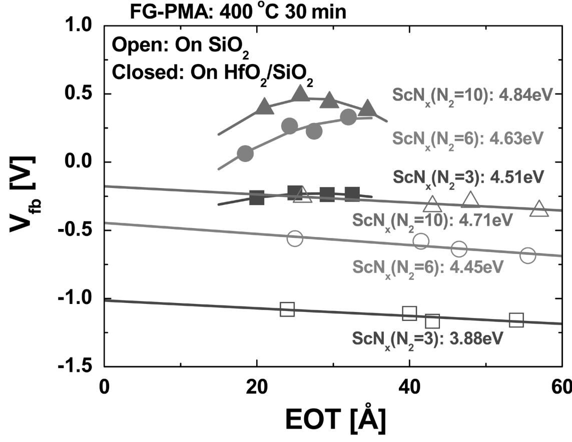

Fig. 7. V_{fb}-EOT relations of ScN_x on SiO_2 and HfO_2 after FG-PMA at 400 °C for 30 min. The ScN_x/SiO_2 samples show a dramatic change of $\Phi_{m,eff}$ with N_2 flow rate. The ScN_x/HfO_2 samples show FLP.

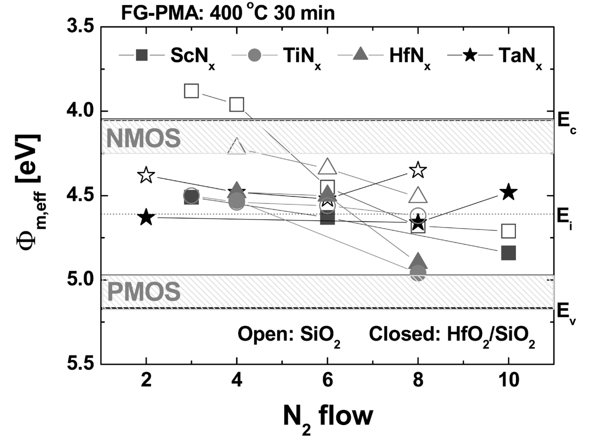

Fig. 8. $\Phi_{m,eff}$ values of binary metal nitrides with various N_2 flow rate. The ScN_x can be used for NMOS with SiO_2. In case of HfO_2, no metal nitride has an appropriate $\Phi_{m,eff}$ value for NMOS.

the SiO_2 samples, the ScN_x/HfO_2 samples show polynomial relations. In the case of the HfO_2/SiO_2 stack, the V_{fb} versus EOT relation is given by

$$V_{fb}=\Phi_{m,eff}-\Phi_s+\frac{1}{2\varepsilon_{SiO_2}}Q_{hk}EOT^2-\frac{1}{\varepsilon_{SiO_2}}(Q_{hk/i}+Q_{hk}T_{SiO_2})EOT+\frac{1}{\varepsilon_{SiO_2}}\left(\frac{1}{2}Q_{hk/i}T_{SiO_2}+Q_{hk}\right)T_{SiO_2} \quad (3)$$

where Q_{hk} and $Q_{hk/i}$ are the bulk charge of the HfO_2 and the charge at the interface between HfO_2 and the interfacial SiO_2 layer, respectively[29]. Eq. (3) is derived under the assumption that Q_{hk} and $Q_{hk/i}$ are significantly higher than the bulk charge of SiO_2 and the SiO_2/Si interfacial charge, respectively. If Q_{hk} is negligible, from Eq. (3), V_{fb} is linearly dependent on the EOT. However, if there is significant Q_{hk}, a second-order polynomial fit to the V_{fb}-EOT data is necessary for the exact determination of $\Phi_{m,eff}$. The $\Phi_{m,eff}$ values of the ScN_x gates on both the SiO_2 and HfO_2/SiO_2 dielectrics were extracted from Eqs. (2) and (3), as shown in Fig. 7. The ScN_x/SiO_2 samples show a wide range of $\Phi_{m,eff}$ values from ~3.9 eV to ~4.7 eV, and NMOS-compatible $\Phi_{m,eff}$ values can be obtained. However, the ScN_x/HfO_2 samples show a relatively narrow range of $\Phi_{m,eff}$ values from ~4.5 eV to ~4.8 eV, and NMOS-compatible $\Phi_{m,eff}$ values cannot be obtained. Fig. 8 shows the extracted $\Phi_{m,eff}$ values of various reactive-sputtered nitrides (ScN_x, TiN_x, HfN_x, and TaN_x) with the N_2 flow rate. All the tested binary metal nitrides on the HfO_2/SiO_2 stacks are inappropriate for NMOS devices.

To evaluate the doping effect of metal gates, TaN, TaC, and TaB_2 sputter targets were used. Fig. 9(a) shows the C-V characteristics of the TaN, TaC, and TaB_2 gates on 46 Å-HfO_2/SiO_2 stacks. In the strong accumulation regime, as shown in Figs. 6 and 9(a), the capacitance values of the TaN sample are nearly the same as those of the Pt sample. However, the capacitance values of the TaC and TaB_2 samples are higher than those of the TaN sample. Fig. 9(b) shows the C-V characteristics of HfN_x gates with various N_2 flow rates. The EOT of the HfN_x sample rapidly increases with the N_2

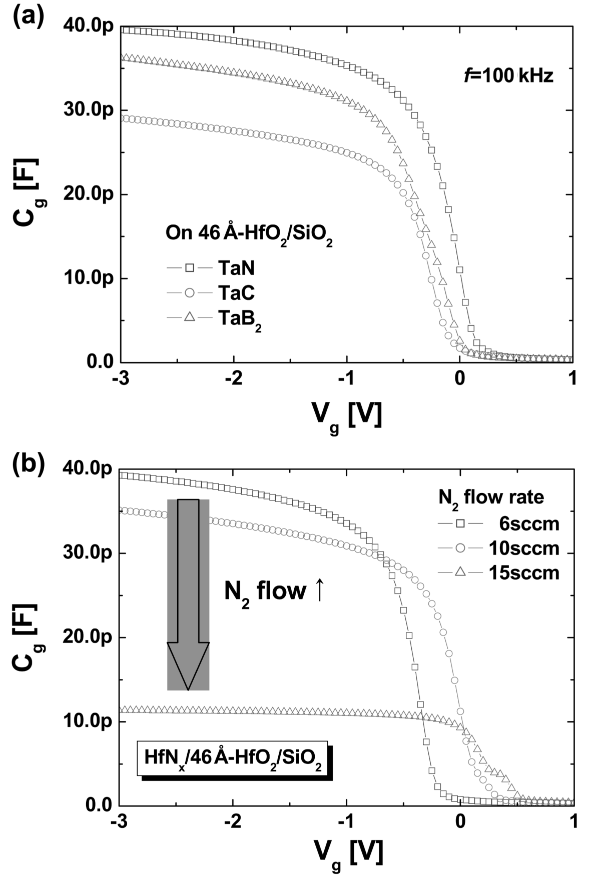

Fig. 9. C-V characteristics of (a) TaN, TaC, TaB_2, and (b) HfN_x gates on 46 Å-HfO_2. The TaC, TaB_2, and HfN_x ($N \geq 10$sccm) gates increase EOT due to excessive C, B, and N, respectively.

flow rate above 10 sccm. The metal HfN has one more electron than needed for a closed shell, and Hf_3N_4 is a dielectric with a closed shell and a band gap[34]. Therefore, the EOT of the HfN_x with an N_2 flow rate above 10 sccm rapidly increases because of excessive nitrogen in the gate. In the same manner, the increased EOT values of the TaC and TaB_2 samples may be due to excessive carbon and boron, respectively. Table 2 summarizes the $\Phi_{m,eff}$ values of the Ta-based materials (Ta, TaN, TaC and TaB_2). Considering the $\Phi_{m,vac}$ values of B (~4.45 eV) and C (~5.0 eV), the excessive boron and carbon may affect the $\Phi_{m,eff}$ values of the TaB_2 and TaC gates, respectively[31]. In an effort to find a means of avoiding excessive doping of carbon, the reactive-sputtered TaC_x gates were evaluated with various CH_4/Ar gas flow rates. As shown in Fig. 10, in contrast to the sample prepared with the TaC target, the EOT values of the reactive-sputtered TaC_x gates are nearly the same as the EOT of the TaN gate. However, as shown in the inset of Fig. 10, midgap $\Phi_{m,eff}$ values were obtained for the TaC_x/HfO_2 samples.

In a recent report, lanthanide (Tb, Er, and Yb)-doped nitrides on SiO_2 were used for NMOS-compatible gates[27]. To evaluate the lanthanide-doped metal nitrides on ALD-HfO_2, TaM_xN_y (M : Dy, Gd, Sm, Tb) gates were deposited by co-sputtering the TaN target with the lanthanide elements. Fig. 11 shows the C-V characteristics of TaN and $TaDy_xN_y$ gates on SiO_2 dielectrics with various thicknesses. In the strong accumulation regime, the capacitance values of the $TaDy_xN_y$ samples are nearly the same as those of the TaN samples. This indicates that the proper addition of Dy does not increase the EOT. The $TaDy_xN_y$ gates on SiO_2 show a lower $\Phi_{m,eff}$ value than that of TaN. Fig. 12 shows the values of both Q_{fixed} in SiO_2 and Q_{hk} and $Q_{hk/i}$ in HfO_2/SiO_2 stacks. The lanthanide elements in the TaM_xN_y gates increase the positive Q_{fixed} in the SiO_2 samples and decrease the magnitude of the negative Q_{hk} and $Q_{hk/i}$ in the HfO_2/SiO_2 samples, compared with the values of the TaN samples. Therefore, the elements may generate positive charges in both SiO_2 and the HfO_2/SiO_2 stack and compensate the negative charges of the TaN/HfO_2 samples. The physical origin of the positive Q_{fixed} may be oxygen vacancies in the dielectrics generated by oxygen transport across the metal/oxide interface. The lanthanide elements may strongly attract oxygen due to their high oxygen reactivity. Fig. 13 shows the extracted $\Phi_{m,eff}$ values of TaM_xN_y gates versus the values of Q_{fixed}. In the case of SiO_2, the $\Phi_{m,eff}$ values of TaM_xN_y are lower than the $\Phi_{m,eff}$ value of TaN for Q_{fixed} values less than $\sim 10^{12} cm^{-2}$ due to the

Table 2. $\Phi_{m,eff}$ values of Ta, TaN, TaC, and TaB_2 gates on SiO_2 and HfO_2

$\Phi_{m,eff}$ [eV]	SiO_2	HfO_2
Ta	4.26	4.50
TaN	4.46	4.52
TaC	4.69	4.78
TaB_2	4.47	4.42

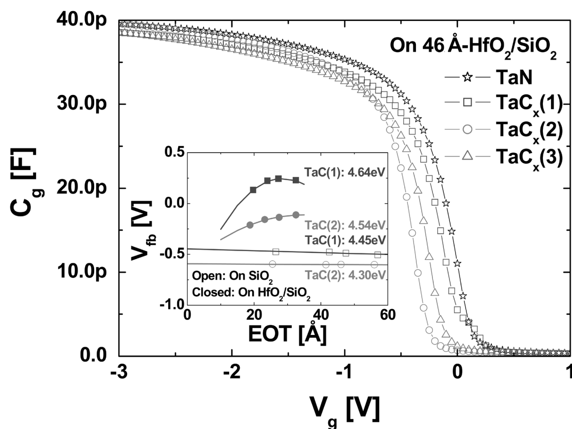

Fig. 10. C-V and V_{fb}-EOT characteristics of TaC_x by reactive sputtering with various CH_4/Ar gas flow rates. The EOT of the TaC_x sample was nearly the same as that of the TaN sample.

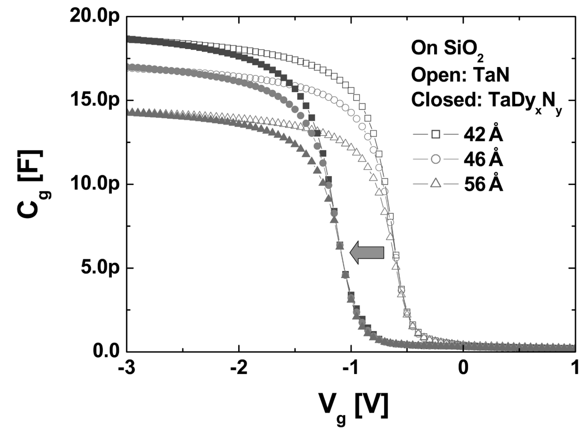

Fig. 11. C-V characteristics of TaN and $TaDy_xN_y$ gates on SiO_2. The $\Phi_{m,eff}$ of $TaDy_xN_y$ is lower than TaN due to the low $\Phi_{m,vac}$ of Dy.

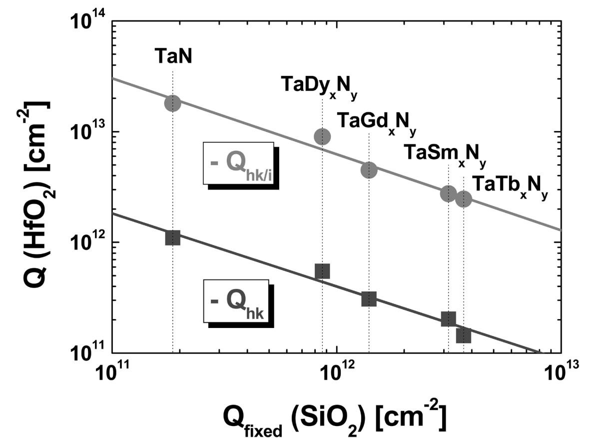

Fig. 12. For the TaN and TaM_xN_y samples, Q_{hk} and $Q_{hk/i}$ in HfO_2 are plotted with Q_{fixed} in SiO_2. The lanthanide elements may generate positive Q_{fixed} and compensate the negative charges of TaN/HfO_2.

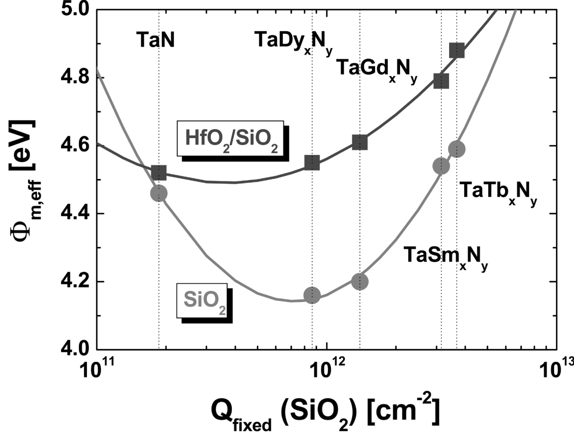

Fig. 13. $\Phi_{m,eff}$ values of the TaN and TaM_xN_y samples versus Q_{fixed} in SiO_2. Compared with the SiO_2 samples, an NMOS-compatible $\Phi_{m,eff}$ value can not be obtained for the HfO_2/SiO_2 samples.

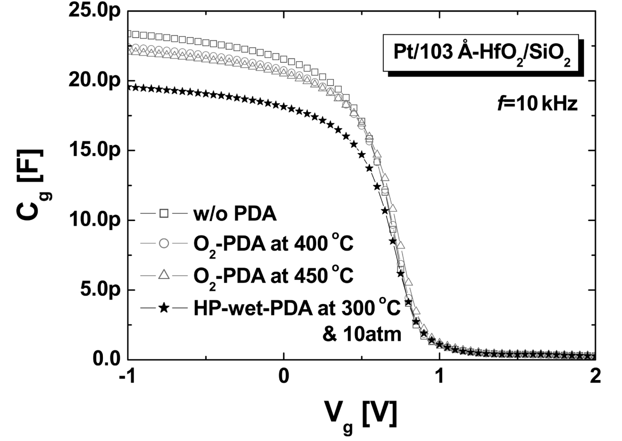

Fig. 15. C-V characteristics of Pt/HfO_2 samples after conventional O_2-PDA and HP-wet-PDA.

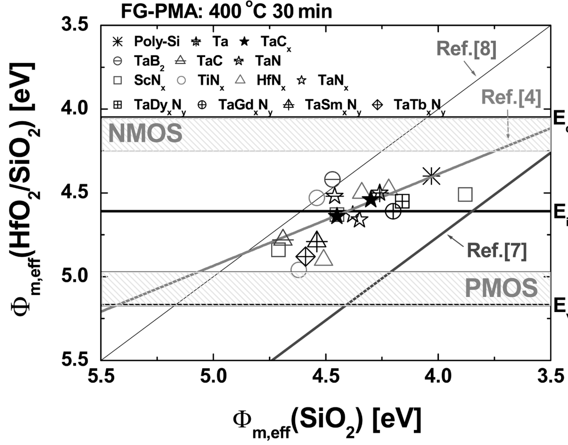

Fig. 14. $\Phi_{m,eff}$ values of all the tested metal gates on HfO_2/SiO_2 stacks versus on SiO_2. No metal is appropriate for NMOS devices with HfO_2.

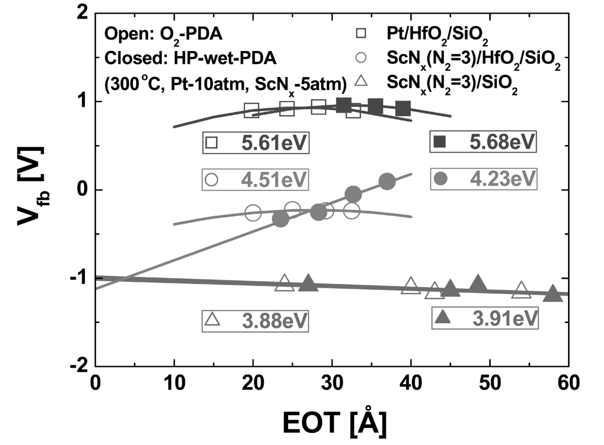

Fig. 16. V_{fb}-EOT relations of the Pt and ScN_x (N_2=3sccm) gates after O_2-PDA and HP-wet-PDA. The HP-wet-PDA on the ScN_x/HfO_2 samples results in a dramatic change of $\Phi_{m,eff}$.

very low $\Phi_{m,vac}$ values (~3 eV) of the lanthanide elements[31]. Therefore, an NMOS-compatible $\Phi_{m,eff}$ can be obtained by using the TaM_xN_y gates on SiO_2. However, the excessive oxygen in the TaM_xN_y may increase the $\Phi_{m,eff}$ value for the Q_{fixed} above ~10^{12}cm^{-2}. Compared with SiO_2, the TaM_xN_y/HfO_2 samples show less reduction of the $\Phi_{m,eff}$ value and an NMOS-compatible $\Phi_{m,eff}$ cannot be obtained. This may be due to the large amount of transported oxygen in the TaM_xN_y gate on HfO_2.

Fig. 14 shows the $\Phi_{m,eff}$ values of all the tested metal gates. All the metals on the HfO_2/SiO_2 stack with the conventional O_2-PDA are inappropriate for NMOS devices. To obtain an NMOS-compatible $\Phi_{m,eff}$, we evaluated various surface treatments on ALD-HfO_2/SiO_2 stacks. Fig. 15 shows the C-V characteristics of Pt gates on 103 Å-HfO_2 dielectrics with conventional O_2-PDA and HP-wet-PDA processes. The PDA processes increase EOT due to the growth of interfacial SiO_2. Fig. 16 shows the V_{fb}-EOT relations of the Pt and ScN_x (N_2=3sccm) samples with conventional O_2-PDA and HP-wet-PDA. For the Pt/HfO_2 and ScN_x/SiO_2 samples, HP-wet-PDA has a negligible effect on the $\Phi_{m,eff}$ value. However, the $\Phi_{m,eff}$ value of the ScN_x gate on HfO_2 significantly depends on the PDA processes, and the HP-wet-PDA dramatically shifts $\Phi_{m,eff}$ towards an NMOS-compatible value. Fig. 17 shows the C-V characteristics of ScN_x/46 Å-HfO_2 samples with various wet-solution (TMAH, H_2O_2, and NH_4OH) treatments after conventional O_2-PDA. There is no additional increase of the EOT by the treatments. Fig. 18 shows the V_{fb}-EOT relations of the ScN_x/HfO_2 samples with various wet-solution treatments. As shown in Figs. 16 and 18, all the wet treatments on the HfO_2 surface result in NMOS-compatible $\Phi_{m,eff}$ values between ~3.95 eV and ~4.23 eV. Table 3 summarizes the Q_{hk} and $Q_{hk/i}$ values of the ScN_x/HfO_2 samples with various wet-solution treatments. The lin-

Fig. 17. C-V characteristics of ScN_x/HfO_2 samples with various wet-solution treatments after O_2-PDA. The EOT is nearly independent of the wet-solution treatments.

Fig. 18. V_{fb}-EOT relations of the ScN_x/HfO_2 samples with various wet-solution treatments. An NMOS-compatible $\Phi_{m,eff}$ between ~3.95 eV and ~4.2 eV can be obtained.

ear V_{fb}-EOT relation of the ScN_x/HfO_2 samples with the HP-wet-PDA at 300 °C and 5 atm in Fig. 16, implies a negligible Q_{hk}. In addition, the process condition yields the lowest $|Q_{hk/i}|$ value of ~$7\times10^{12}cm^{-2}$, which is similar to the value of the Pt/HfO_2 sample (~$6\times10^{12}cm^{-2}$). A high $Q_{hk/i}$ value is generally observed in the HfO_2/SiO_2 stack.[29] Fig. 19 shows the V_{fb}-EOT relations of the ScN_x (N_2=6sccm) and HfN_x (N_2=4sccm) gates on HfO_2 with and without TMAH treatments. From Figs. 16, 18, and 19, coexistence of nitrogen deficiency in ScN_x and oxygen deficiency in HfO_2 might cause significant extrinsic pinning states which might be related to the Sc-Hf bonds at the ScN_x/HfO_2 interface.

4. CONCLUSIONS

Using both ScN_x gates and wet surface treatments on ALD-HfO_2, as shown in Fig. 20, NMOS-compatible $\Phi_{m,eff}$ values of ~ 4 eV were obtained. Therefore, the wet treatment is a promising process technology to reduce the extrinsic FLP, especially for NMOS-compatible metal gates.

Table 3. Q_{hk} and $Q_{hk/i}$ of the Pt and ScN_x (N_2=3sccm) on HfO_2. The ScN_x with the HP-wet-PDA at 300 °C and 10 atm results in the excellent quality

Samples ⁄ Charges [cm^{-2}]			$\|Q_{hk}\|$	$\|Q_{hk/i}\|$
Pt		O_2-PDA	**3.5×10^{11}**	**5.7×10^{12}**
ScN_x		O_2-PDA	2.2×10^{11}	3.9×10^{12}
	HP-wet-PDA	200°C 10atm	7.5×10^{11}	1.6×10^{13}
		300°C 10atm	1.1×10^{12}	2.5×10^{13}
		300°C 5atm	**Negligible**	**7.0×10^{12}**
	wet solution	TMAH	7.6×10^{11}	1.7×10^{13}
		H_2O_2	7.0×10^{11}	1.5×10^{13}
		NH_4OH	7.2×10^{11}	1.5×10^{13}

Fig. 19. V_{fb}-EOT relations of the ScN_x (N_2=6sccm) and HfN_x (N_2=4sccm) gates on HfO_2 with and without TMAH treatment.

Fig. 20. Effect of various wet treatments on the $\Phi_{m,eff}$ values of ScN_x. Using ScN_x gates and wet treatments, NMOS-compatible $\Phi_{m,eff}$ values can be obtained.

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