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Schottky Barrier Metal-Oxide-Semiconductor Field-Effect Transistors for Nano-Regime Applications

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Erbium-/platinum-silicided *n*/*p*-type Schottky barrier metal-oxide-semiconductor-field-effect transistors(SB-MOSFETs) were manufactured at various sizes, from 20 μm to 23 nm. The manufactured SB-MOSFETs showed excellent drain induced barrier lowering(DIBL) characteristics due to the presence of a Schottky barrier between the source and the channel. The DIBL and subthreshold swing(SS) characteristics were comparable to the values of ultimate scaling limit of double gate(DG) MOSFETs, which shows the possible application of SB-MOSFETs in the nanoscale regime.

Keywords: Schottky barrier, SB-MOSFETs, erbium-silicide, platinum-silicide, scaling, DIBL, subthreshold swing

1. INTRODUCTION

As the gate length of metal-oxide-semiconductor-field-effect transistors (MOSFETs) have been reduced down to the decananometer scale, ultra-shallow junction formation techniques have become of great importance for the suppression of short channel effects[1]. However, one major drawback in the usage of an ultra-shallow junction is the high parasitic series resistance. This obstacle can be overcome with Schottky barrier metal-oxide-semiconductor-field-effect transistors(SB-MOSFETs) by replacing the impurity-doped source and drain regions with silicides[2, 3]. The structure involved is quite simple, and an ultra-shallow junction can be formed easily and accurately with very low parasitic source and low drain resistance. Thus, SB-MOSFETs have been proposed as an alternative to conventional MOSFETs for sub-100 nm applications[2, 3].

This paper reports on an analysis of the short channel characteristics of SB-MOSFETs using DIBL and SS characteristics. In addition, a simple DIBL model of SB-MOSFETs is proposed and compared with the scaling theory of DG-MOSFETs.

2. EXPERIMENTAL PROCEDURE

As starting materials, (100) boron-doped *p*-type and phosphorus-doped *n*-type silicon-on-insulator (SOI) wafers were used for *n*/*p*-type SB-MOSFETs. The doping concentration was about 1.0×10^{15} cm^{-3} for both the *n*-type and *p*-type SOI wafers. The thicknesses of the SOI and the buried oxide (BOX) layer were 100 nm and 200 nm, respectively. The gate oxide was 5-nm-thick SiO_2, grown via thermal oxidation, and the gate electrode was highly phosphorus-doped *n*-type polycrystalline silicon. Electron-beam lithography was employed to define the gate pattern. After gate etching, a 30-nm-thick gate sidewall spacer was formed by using a thermal oxidation method. After blanket dry etching of the gate sidewall spacer, 100-nm thicknesses of erbium and platinum were sputtered for *n*-type and *p*-type SB-MOSFETs, respectively. Erbium-silicide and platinum-silicide were formed by using a rapid thermal annealing (RTA) technique. The annealing temperature and annealing time were 500 °C and 5 min, respectively. The non-reacted erbium and platinum were removed by using sulfuric peroxide mixture (SPM) and aqua regia for 10 min, respectively. The formation of $ErSi_{1.7}$ and PtSi phase were confirmed by x-ray diffraction (XRD) and Auger electron spectroscopy (AES) analysis. The sheet resistances were less than 30 Ω/□ and 10 Ω/□ for erbium-silicide and platinum-silicide, respectively, even when the line width was less than 100 nm. Thus, erbium and platinum are applicable for manufacturing SB-MOSFETs in the sub-100 nm regime.

3. RESULTS AND DISCUSSION

Figure 1 shows the SEM (a) and TEM (b) images of the

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manufactured long channel *n*-type SB-MOSFETs. It is clearly shown that erbium-silicide is selectively grown on the silicon region and the non-reacted erbium is perfectly removed.

Figure 2 shows the I_{DS}-V_{GS} characteristics of the 20-μm-long channel *n/p*-type SB-MOSFETs. The thicknesses of the gate oxide and the spacer are 5 nm and 15 nm, respectively. Both *n/p*-type SB-MOSFETs show a high on/off current ratio, of larger than $I_{on}/I_{off}>10^5$, along with a low leakage current ($I_{LKG}<100$ pA/μm). The values of the on/off ratio and the leakage current level were the highest and lowest, respectively, compared with previously published data on *n*-type SB-MOSFETs[2]. In addition, the DIBL was almost completely suppressed in both *n/p*-type SB-MOSFETs, and the SS value was 60 mV/decade in the *n*-type SB-MOSFETs.

Figure 3 shows the I_{DS}-V_{GS} characteristics of erbium-silicided 100-nm gate length *n/p*-type SB-MOSFETs, which also showed excellent short channel characteristics. The measured SS and DIBL values were 70 mV/decade and 30 mV, respectively, for the *n*-type SB-MOSFETs.

Figure 4 shows the I_{DS}-V_{GS} characteristics of 23-nm gate length *n*-type SB-MOSFETs. Although the substrate boron doping concentration was 10^{15} cm^{-3}, the short channel effect was sufficiently suppressed, due to the presence of the Schottky barrier between the source and the channel. The existence of interface traps can severely affect the short

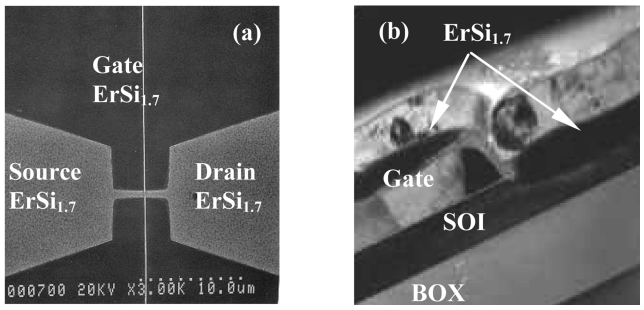

Fig. 1. SEM and TEM images of the erbium-silicided *n*-type SB-MOSFET.

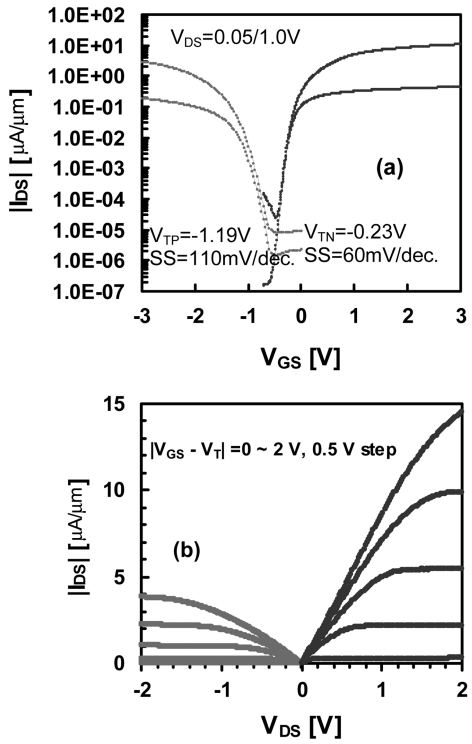

Fig. 2. I_{DS}-V_{GS} (a) and I_{DS}-V_{DS} (b) characteristics of a 20-μm long channel *n/p*-type SB-MOSFET.

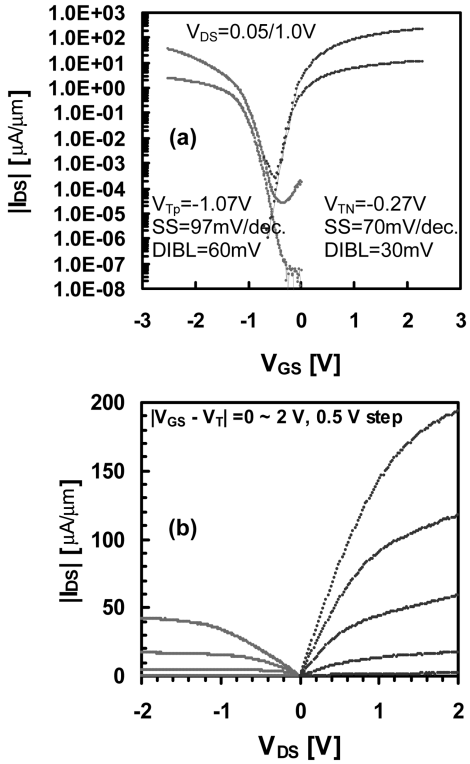

Fig. 3. I_{DS}-V_{GS} (a) and I_{DS}-V_{DS} (b) characteristics of a 100-nm gate length *n/p*-type SB-MOSFET.

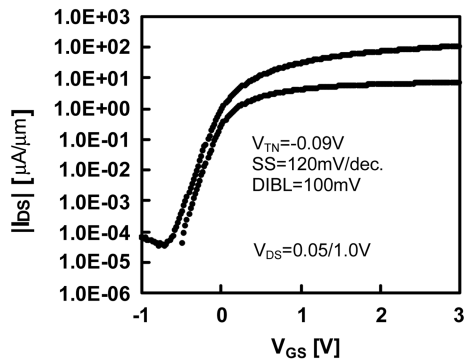

Fig. 4. I_{DS}-V_{GS} characteristics of a 23-nm *n*-type SB-MOSFET.

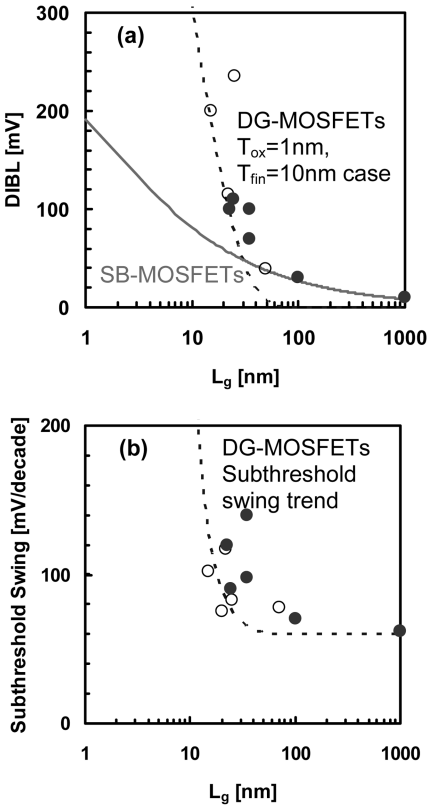

Fig. 5. DIBL (a) and Subthreshold Swing (b) characteristics of SB-MOSFETs.

channel characteristics in SB-MOSFETs, especially for low-doped substrates, because of the severe penetration of drain field into the source/channel interface. The penetration of drain field can cause an interface trap mediated leakage current, leading to a degradation of the SS value and to leakage current characteristics.

Figure 5 shows the DIBL (a) and SS (b) characteristics of the SB-MOSFETs with various gate lengths. In Fig. 5(a), the solid and dotted lines represent the theoretical DIBL characteristics of SB-MOSFETs and DG-MOSFETs, respectively; in addition, the open circles are plotted based on published data[2], and the closed circles are the data from this work. The scaling theory of DG-MOSFETs can be found in[4]. In the calculations of the DIBL in the DG-MOSFETs, the gate oxide and body thicknesses were assumed as 1 nm and 10 nm, respectively. Note that these assumed values correspond to the ultimate minimum values in device technology. The DIBL characteristics of the SB-MOSFETs are superior to those of DG-MOSFETs, which is due to the presence of the Schottky barrier between the source and the channel. In DG-MOSFETs, the subthreshold characteristics, including DIBL and SS, are mainly determined by the built-in potential. In short-channel devices, as the drain voltage increases, the built-in potential between the source and the channel decreases, resulting in a DIBL effect. However, in SB-MOSFETs, the Schottky barrier mainly determines the subthreshold characteristics. Thus, the DIBL characteristics of SB-MOSFETs can be described by the Schottky barrier lowering due to the drain voltage. In SB-MOSFETs, a decrease in threshold voltage corresponding to an increase in drain voltage, as caused by the Schottky barrier lowering, can be expressed as follows.

$$\Delta V_T = \sqrt{\frac{q}{4\pi\varepsilon}}\left[\sqrt{\frac{V_{DS}^{H}}{L_{eff}}} - \sqrt{\frac{V_{DS}^{L}}{L_{eff}}}\right]$$

In the above equation, L_{eff} refers to the effective gate length, and V_{DS}^{H} and V_{DS}^{L} refer to high and low drain voltage, respectively.

In Fig. 5(b), the dotted line represents the theoretical SS characteristics of DG-MOSFETs, with a 1-nm gate oxide and a 10-nm body thickness. As shown, the SS characteristics of SB-MOSFETs are nearly comparable to ultimately scaled DG-MOSFETs.

4. CONCLUSION

In this study, SB-MOSFETs were manufactured, and their electrical characteristics were analyzed. In SB-MOSFETs, the DIBL is strongly suppressed, due to the presence of a Schottky barrier between the source and the channel. The DIBL and SS characteristics of SB-MOSFETs are comparable to the values of ultimately scaled DG-MOSFETs, which shows the possible application of SB-MOSFETs in the nanoscale regime as an alternative to conventional MOSFETs.

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