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Metal Gate and High-k Gate Dielectrics for sub 50 nm High Performance MOSFETs

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Over the past few years, metal gates and high-k gate dielectrics have been intensively developed to implement sub 50nm CMOS technology. Nevertheless, some issues of metal gate and high-k gate dielectric need to be solved. In particular, the high density of traps in dielectric and workfunction modulation with metal gate should be addressed by either understanding the mechanism or developing a new process. In this paper, we propose an analyses method and various processes to understand and solve the problems of metal gate and high-k gate dielectrics. First, to effectively passivate high-k/Si interface traps, post metallization annealing in high pressure hydrogen ambient was investigated. Compared with conventional forming gas annealing, high pressure annealing showed improved device performance owing to the effective passivation of interface traps. Second, the effect of traps in the high-k layer was evaluated by single pulsed I_d-V_g measurement and reliability such as bias temperature instability. By using nano-scale analysis, we have confirmed that non-uniform oxygen vacancy causes charge trapping and reliability degradation. Then, the interaction of metal gate and gate dielectric during thermal process was investigated with various metal electrodes and systems. Metal/dielectric interaction was found to be severe in elemental and ternary metal electrodes, while the binary metal electrode showed minimum interaction. To achieve appropriate workfunction with minimal interaction, the bi-layer metal electrode and conducting oxide electrode were developed. Both electrodes showed suitable workfunction which is close to conduction and valance band of silicon with improved thermal stability.

Key words: high-k gate dielectrics, metal gate electrodes, high pressure post metallization annealing, charge trapping, oxygen vacancy

1. INTRODUCTION

To achieve high performance sub-50nm transistor, aggressive scaling of gate oxide and minimization of poly depletion effect seem to be inevitable [1]. For past few years, many reports have been made on high-k materials and metal gate electrodes to reduce gate leakage current and remove the poly depletion effect. First, in order to reduce the gate leakage current, replacement of SiO_2 with high-k materials seems to be inevitable in sub-1nm oxide thickness regime. By using high-k materials, electrical oxide thickness can be further scaled while physical thickness can be increased due to high dielectric constants. Among the high-k materials, HfO_2 and its silicate are the most outstanding materials due to their relatively high dielectric constant (10~20), large band gap, and compatibility with the conventional CMOS process. For that reason, physical and electrical characteristics of hafnium (Hf) based dielectrics have been intensively studied [2-4]. However, the high density of interface traps and fixed charges in the high-k oxide are major obstacles for the formation of a high quality high-k oxide. In that sense, the understanding of trap generation mechanisms and the development of new process for trap passivation must be are also needed.

Another approach to overcome the limitations of feature size scaling is the replacement of the poly-silicon gate to metal gate electrode since the poly depletion effect and the increased resistance of the poly-silicon electrode degrades the scalability of the inversion oxide thickness and circuit performance in an ultra-thin oxide regime. In addition, when poly silicon is deposited on the high-k gate dielectrics, a significant threshold voltage shift was observed due to Fermi level pinning (FLP)[5-6]. Recently, many reports with various materials have been published to find proper effective workfunctions which are close to conduction and valence band of silicon substrate. Many of the reports on metal gate electrodes focus on metal gate workfunction adjustment without considering metal/high-k interaction issues. However, to realize a high performance device with good reliability, the effects of metal/high-k stack interaction should be considered when a metal gate electrode is developed.

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In this paper, we discuss the process and structure optimization for a high performance sub 50nm transistor. In the first section, the high pressure post metallization annealing is demonstrated as an effective high-k/Si interface passivation technique. In the second section, we discussed the impact of an oxide trap site on charge trapping and reliability. With analyses of high-k gate dielectrics in the nano-scale area, we proposed the optimized post deposition annealing process for passivation of oxygen vacancy in a high-k layer. In the last section, the impact of the metal/dielectric interaction depending on the metal electrode system and thermally stable workfunction modulation method has been realized by the modification of structure and materials.

2. RESULT AND DISCUSSION

2.1. Effective passivation of a high-k dielectric/Si interface trap by high pressure post metallization annealing

It is known that forming gas annealing around 400°C is sufficient to passivate the SiO_2/Si interface states. For that reason, forming gas annealing was used for the interface trap passivation technique at the end of the wafer process. In the case of high-k gate dielectrics, high temperature (up to 600°C) FGA seems to be necessary to efficiently passivate the high-k/Si interface traps [7-8]. Considering back end processes, such as the interconnect process, post-metallization annealing in high temperatures (higher than 500°C) may not be compatible with the standard CMOS flow.

To enhance the rate of interface passivation at low temperature, post metallization annealing in high pressure ambient was developed. As expected, samples annealed in the high pressure hydrogen ambient showed the higher passivation rate of the interface state. The MOSFET with high-k gate dielectric showed improvement in the linear drain current (I_d) and transconductance (g_m) (Fig. 1). To find the most effective annealing ambient, high pressure post metallization annealing was performed in various gas ambient. Inset of Fig. 1 summarizes the g_m improvement after high pressure annealing. After high pressure nitrogen and forming gas annealing, negligible improvement of g_m was observed, while significant g_m improvement was observed after high pressure pure hydrogen annealing. Based on this result, it could be concluded that post metallization anneal in high pressure hydrogen ambient seems to be the most effective way to maximize the device performance.

The interface states density (N_{it}) of high pressure annealed samples was measured by the fixed-amplitude charge pumping method (Fig. 2)[9]. After high pressure annealing, a significant reduction of interface state was observed. Also, as increasing annealing pressure, a further decrease of the interface state was observed. The further reduction of N_{it} after high pressure annealing indicates that interface traps at a high-k/Si interface still remain after conventional forming gas annealing. The improvement of the drain current and transconductance in Fig. 1 can be attributed to the effective passivation of an interface trap at a high-k dielectric and Si substrate.

The effect of high pressure annealing depending on the surface preparation method and post deposition anneal method was investigated with various types of high-k dielectrics. Figure 3 shows the change of transconductance after high pressure annealing. All types of high-k gate dielectrics showed improvement in transconductance, regardless of process conditions. In addition, samples with nitrogen related processes, such as surface nitridation and nitrogen PDA, showed a further improvement than non-nitrogen related processes. These results suggest that high pressure

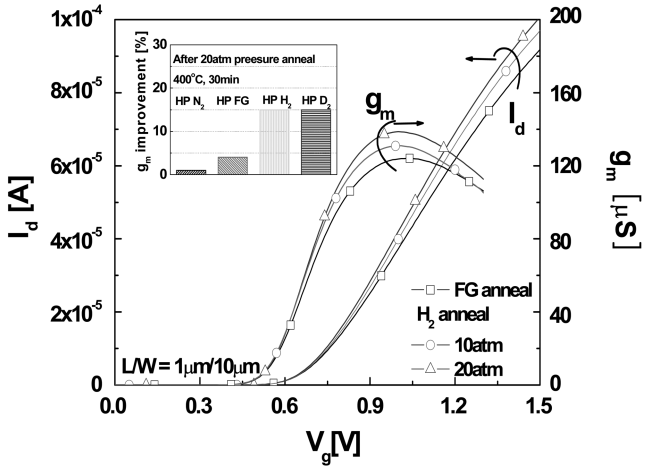

Fig. 1. The liner drain current (I_d) and transconductance (g_m) versus the gate voltage (V_g) plot of conventional forming gas annealed and high pressure annealed HfAlO/Hf-silicate nMOSFET. The inset figure shows g_m improvement after high pressure anneal depending on gas ambient.

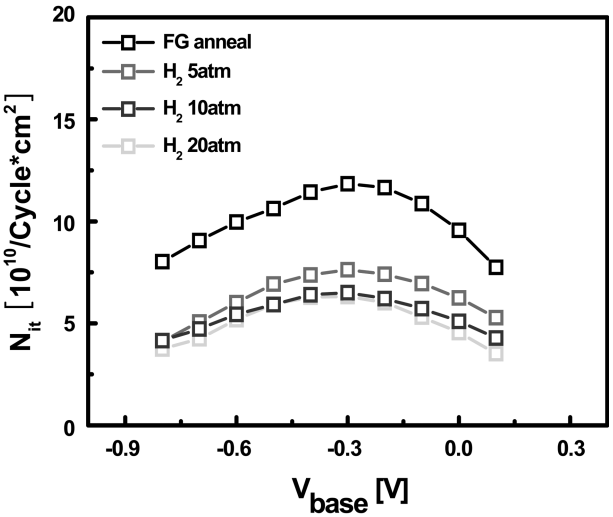

Fig. 2. The interface state densities (N_{it}) of HfAlO/Hf-silicate nMOSFET measured with a fixed amplitude charge pumping method.

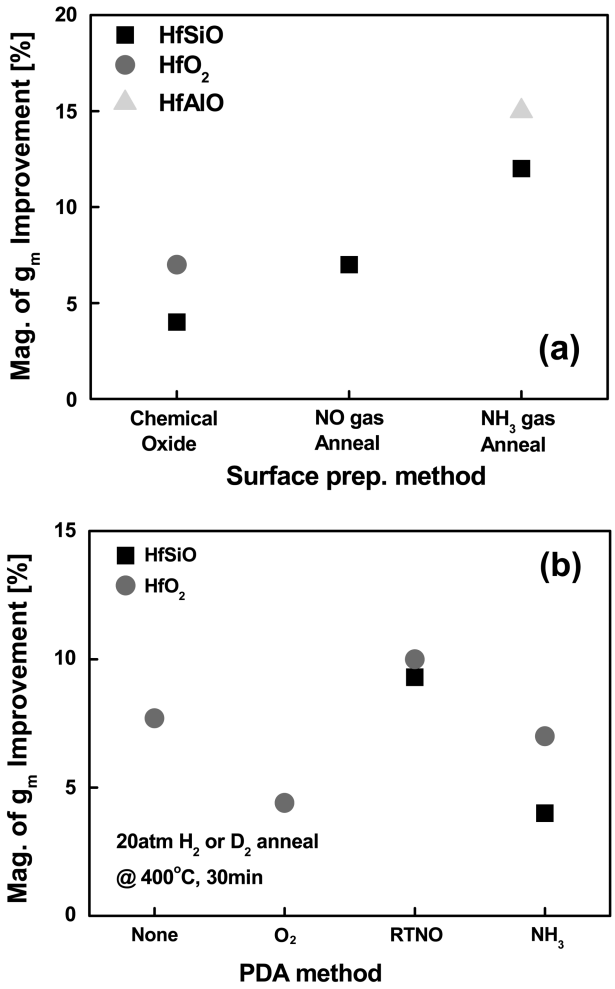

Fig. 3. The effect of high pressure post metallization annealing depending on (a) surface preparation method and (a) PDA method. Annealing was performed at 400°C temperature for 30 minutes in 20 atm pressure.

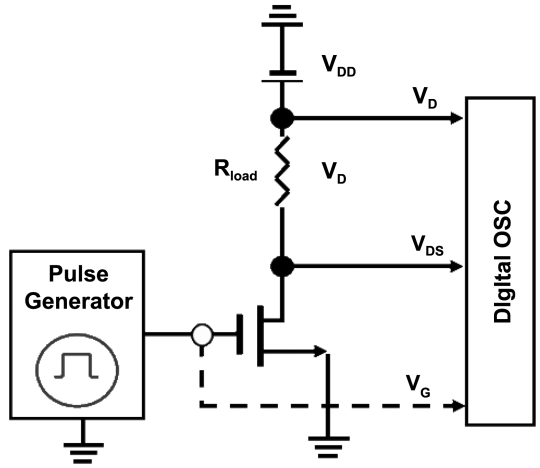

Fig. 4. A schematic diagram for single pulsed I_d-V_g measurement.

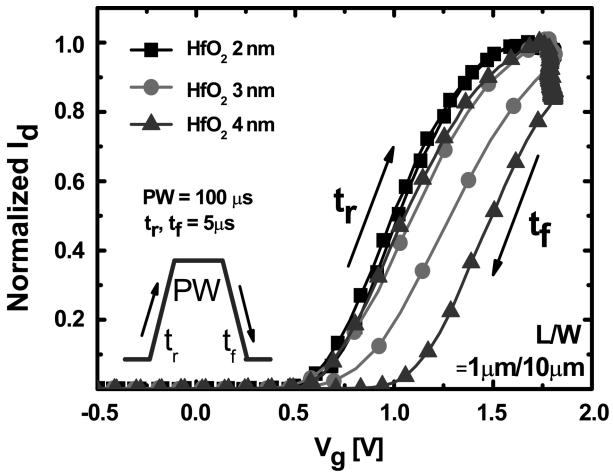

Fig. 5. Normalized pulsed I_d-V_g characteristics depending on the physical HfO_2 thickness. Large hysteresis of V_{th} was observed when HfO_2 thickness increased.

annealing is more effective for nitrogen related trap passivation. Compared with a conventional forming gas annealed sample, the MOSFETs annealed in high pressure ambient exhibits significantly reduced interface traps, which can lead to a significant improvement of high-k dielectric/Si interface.

2.2. The effect of oxygen vacancy in hafnium oxide on electrical and reliability characteristics

To implement high-k gate dielectrics in a CMOS device, high quality dielectric should be achieved. Up to now, one of major concerns of high-k dielectrics has beeb the high density of the fixed charge [10-13] since it causes significant charge trapping as well as threshold voltage instability, which usually leads to the degradation of device performance and reliability [14-16]. Without a clear understanding of the effects of the fixed charge, a high performance transistor with good reliability cannot be achieved. In this section, we will discuss the impacts of a charge trapping on the electrical characteristics of HfO_2 MOSFETs with a single pulsed I_d-V_g measurement, and we will investigate the origin of the fixed charge with a nano-scale area measurement.

As discussed above, charge trapping through the trap site in a high-k dielectric is the root cause of threshold voltage instability and it degrades device reliability. To estimate the initial charge trap site in a high-k gate dielectric, fast measurement using a microsecond single pulse was proposed [17-18]. Figure 4 shows a schematic diagram of a single pulsed I_d-V_g measurement. In stead of a DC voltage sweep, a single pulse applied to the gate and measured voltage change at the R_{load} to estimate the drain current. By using a single pulsed I_d-V_g measurement, a different physical thickness of HfO_2 was characterized (Fig. 5). As the physical thickness of HfO_2 become thicker, a single pulsed I_d-V_g measurement showed a further increase of hysteresis. The increase of hysteresis in a

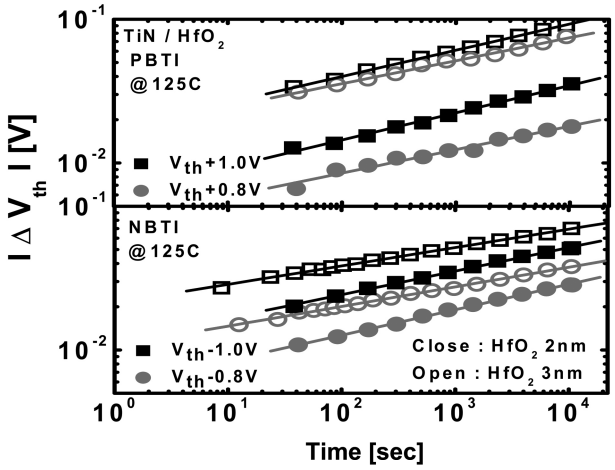

Fig. 6. Bias Temperature Instability (BTI) characteristics of HfO_2 depending on the dielectric thickness. As HfO_2 thickness is scaled down, a reduced V_{th} shift was observed under BTI stress.

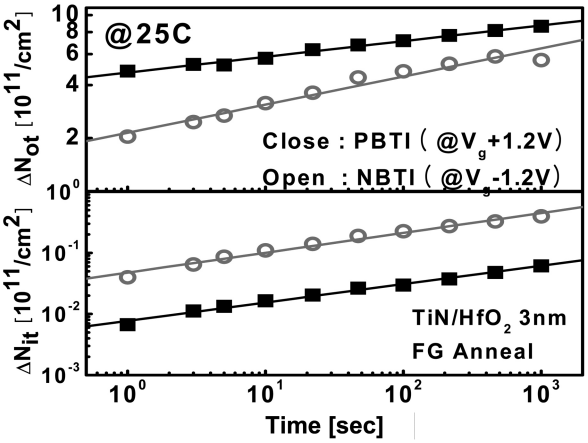

Fig. 7. N_{ot} and N_{it} generation behavior during BTI results. N_{ot} and N_{it} were extracted from V_{th} shift ($N_{ot}=C_{ox}V_{th}/q$) and charge pumping (CP) measurement ($N_{it}=I_{cp}/qfA$), respectively.

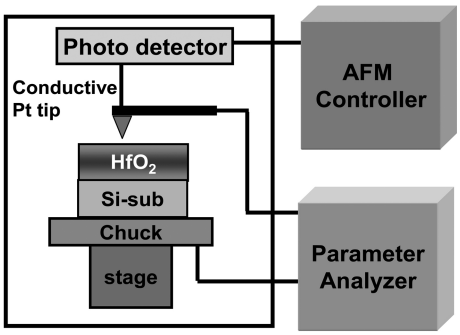

Fig. 8. A schematic diagram of conducting AFM. A semiconductor parameter analyzer was connected for accurate current measurement. A platinum (Pt) coated Si cantilever was used as a nano size tip.

thick oxide can be understood by the increased trap site in the high-k layer [19-20]. This result indicates that the oxide trap

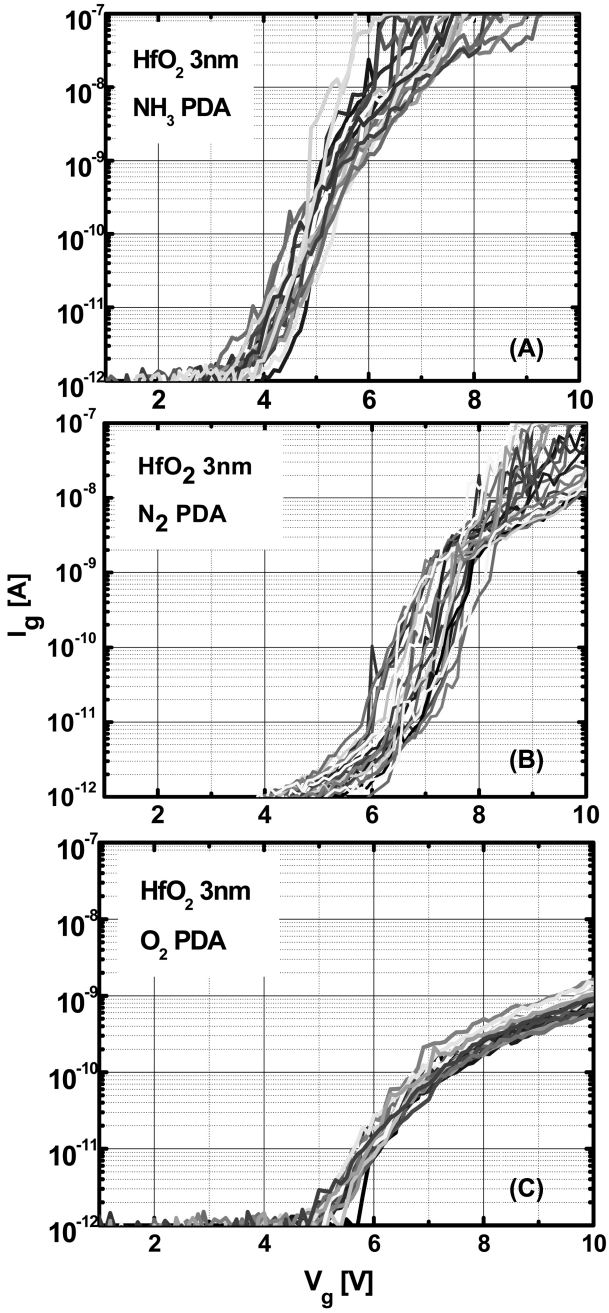

Fig. 9. I-V characteristics of 3 nm HfO_2 depending on PDA ((a) NH_3, (b) N_2, and (c) O_2). All samples received the same thermal budget at 700C for 1min.

density wass proportionally increased when the physical thickness of high-k layer was increased. To minimize the trap density, either scaling of the physical thickness or optimization of dielectric formation process is need. To understand the effect of the physical thickness on device reliability, the Bias Temperature Instability (BTI) characteristics of the HfO_2 transistor depending on physical thickness were investigated (Fig. 6). Compared with thick HfO_2 oxide, thin HfO_2 showed the improved BTI characteristics. This is

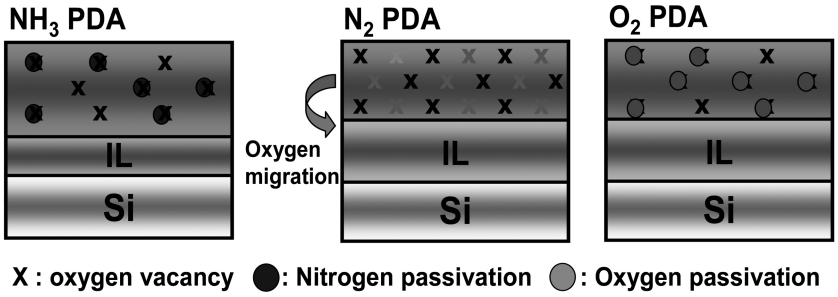

Fig. 10. Diagram of oxygen vacancy passivation and the generation mechanism during PDA.

attributed to the reduction of the available charge trap site as the HfO_2 thickness becomes thinner. To clearly understand the role of traps in the HfO_2 layer, charge pumping (CP) was performed to observe the interface trap generation during BTI stress (Fig. 7). The generation rate of N_{it} is significantly lower than that of N_{ot}. This also indicates that traps in HfO_2 bulk are the dominant degradation source rather than the interface traps during BTI stress.

To understand the origin of traps in HfO_2, nano-scale reliability characteristics were evaluated by conducting atomic force microscopy (C-AFM). In this experiment, to measure the wide range of leakage current with accuracy, source and measure unit (SMU) in Agilent 4155 was connected to the AFM system (Fig. 8). Also, to avoid the damage of Pt coated Si cantilever from ionic contamination during measurement, electrons are injected from the substrate[21]. Figure 9 shows the nano-scale I-V characteristics of HfO_2 depending on the post deposition annealing (PDA). A wide distribution of gate leakage current was observed in HfO_2 with N_2, and NH_3 PDA. However, compared with N_2 PDA, NH_3 PDA showed a reduction of gate leakage current non-uniformity. The significant reduction of gate leakage current non-uniformity was observed when the sample was annealed in O_2 ambient. These results suggest that nitrogen incorporation helps to reduce gate leakage current variation, but it cannot fully passivate the traps in HfO_2. Only with oxygen incorporation, traps in HfO_2 can be successfully passivated.

Gate leakage current variation in the nano-scale area can be understood with Fig. 10. During NH_3 and O_2 PDA, nitrogen and oxygen incorporated into HfO_2 dielectric and passivate trap sites. However, during N_2 PDA, only oxygen migration occureded due to the inert property of N_2 gas. Thus, a wide variation of gate leakage current was observed in N_2 PDA because of the increased oxygen vacancy site in the HfO_2 layer. Based on these results, it is concluded that careful optimization of dielectric formation process is necessary to aachieve a high performance HfO_2 transistor with good reliability.

The effects of oxygen vacancy passivation on charge trapping and reliability were evaluated by single pulsed I_d-V_g measurement and BTI characteristics. Figure 11 shows the

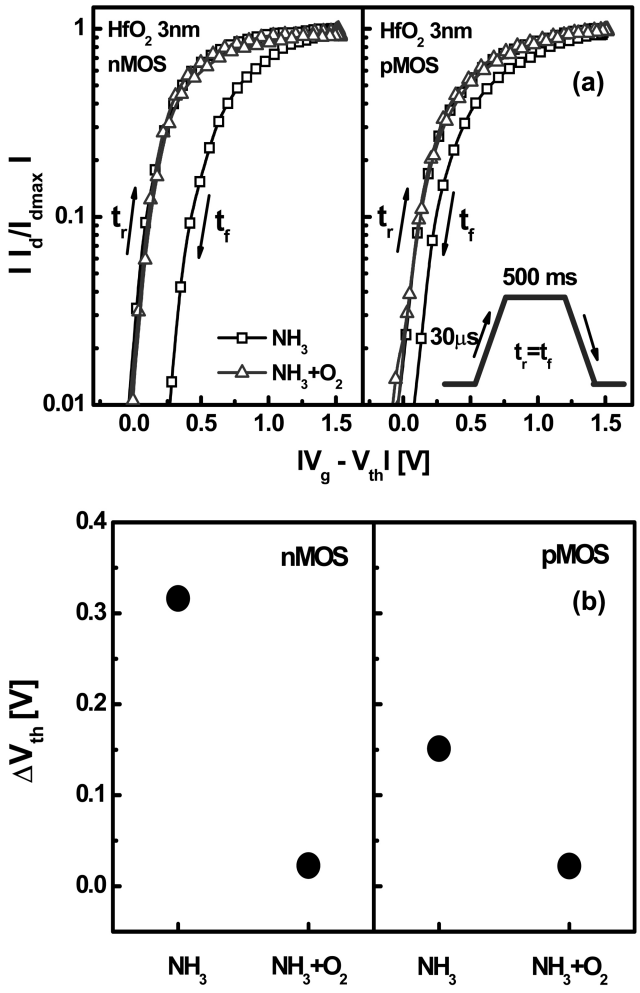

Fig. 11. (a) Single pulsed I_d-V_g characteristics with NH_3 and NH_3 + O_2 PDA treatment. (b) Summary of V_{th} hysteresis during single pulsed I_d-V_g measurement. O_2 PDA followed by NH_3 PDA showed a significant reduction of charge trapping in n and pMOSFET, respectively.

single pulsed I_d-V_g characteristics depending on PDA treatment. Comparing NH_3 PDA, O_2 PDA followed by NH_3 PDA showed a reduction of V_{th} hysteresis in both n and pMOSFET, respectively. The change of reliability after O_2

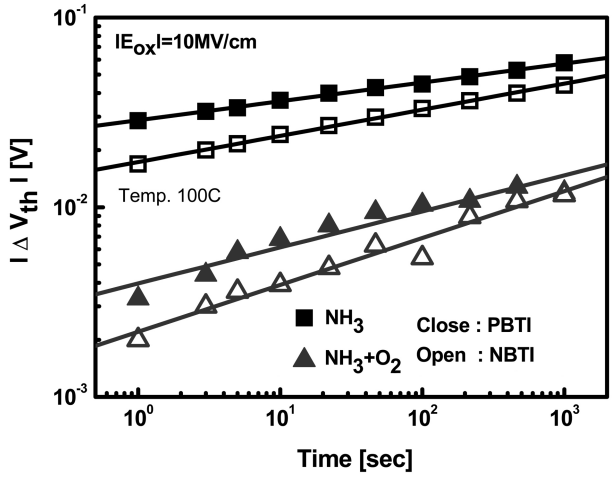

Fig. 12. Positive and negative bias temperature instability characteristics depending on PDA treatment under 10MV/cm stress.

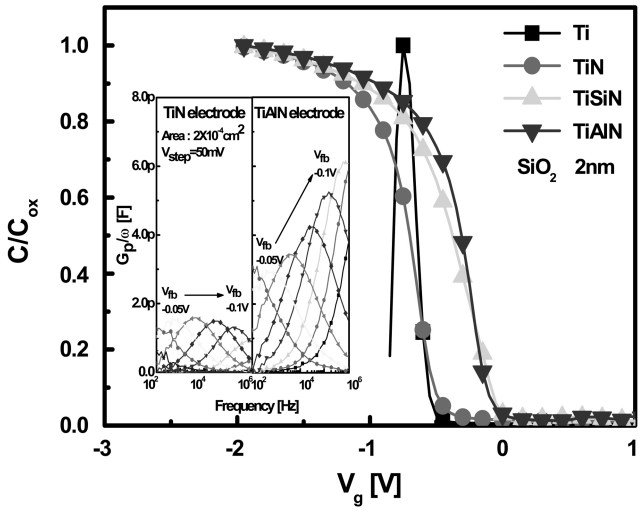

Fig. 13. CV characteristics of a Ti-based electrode capacitor. The inset figure shows a conductance loss peak of TiN, TiAlN electrode capacitor. TiAlN showed higher interface trap densities than TiN (High G_p/w value).

PDA is shown in Fig. 12. The additional O_2 PDA sample showed reduced initial charge trapping as well as V_{th} shift under BTI stress. The reduction of V_{th} hysteresis in a single pulsed I_d-V_g measurement and V_{th} shift in BTI reliability can be explained by the passivation of the oxygen vacancy in HfO_2.

A C-AFM study of HfO_2 showed that the nano-scale non-uniformity of gate leakage current strongly depends on the PDA conditions. Smaller leakage current distribution in nano-scale measurement and improved reliability in MOSFET after oxygen anneal indicates that the oxygen vacancy is a major source of gate leakage current and the origin of the charge trap sites in HfO_2. Thus, the correlation between the reliability characteristics of the HfO_2 transistor such as BTI stress conditions and the oxygen vacancy is clearly demonstrated. To achieve a high performance HfO_2 transistor with a good reliability, the careful passivation of oxygen vacancies are necessary.

2.3. Band edge metal gate candidate materials for NMOS and PMOS application

With the continuous scaling of CMOS devices, metal gates with workfunction (WF) close to the silicon conduction band (~ 4.2 eV) and valance band (~ 5.2 eV) are necessary to replace poly silicon for dual metal gate applications. These NMOS and PMOS candidate materials have different sets of issues. Usually, the NMOS candidates are very reactive with low electronegativity. When NMOS candidate metals contact with dielectric materials, the interaction between metal/dielectric creates interface defect sites, which makes it hard to achieve the desired WF [22].

On the contrary, PMOS metal suffers severe Fermi level pinning and flat band voltage moves towards the mid-gap at a high thermal budget [23]. There are many postulations which cause this kind of pinning effect. Recently, it is mostly believed that the oxygen vacancy created for high-k dielectric is responsible for this phenomenon [24].

In addition, when a metal electrode is developing, the thermal stability of the metal electrode should be also considered together, since, in the conventional CMOS process, high temperature annealing is required to activate source/drain dopants and causes metal/dielectric interaction [25-26]. Thus, the impact of metal electrode/dielectric interaction on the gate oxide reliability should be understood.

In this section, the trap generation behavior influenced by the metal electrode material will be discussed. Then, with based on the understanding of the metal/dielectric interaction, we will propose a thermally stable bi-layer structure electrode and conducting oxide electrode for n, pMOSFET metal gate.

2.3.1. Thermal stability of metal electrodes and its impact on gate dielectric characteristics

To estimate the effect of metal interaction, interface trap generation behavior, which is induced by the metal gate, was studied using capacitors with various titanium-based metal electrodes (Ti, TiN, TiAlN, and TiSiN). CV and conductance data shows that D_{it} is strongly depends on metal electrode species (Fig. 13). Ternary metal-nitrides showed more D_{it} degradation than binary metal-nitride. D_{it} degradation was more pronounced on thin SiO_2 (Fig. 14), suggesting some metals might have reacted with SiO_2 or diffused into SiO_2 and/or Si substrate.

To evaluate metal diffusion into Si substrate, Zerbst measurement was used and correlated with D_{it} (Fig. 15) [27]. Elemental Ti, Mo electrode samples exhibited shorter minority carrier generation time ($\tau_{minor.}$) and high D_{it} values, indicating

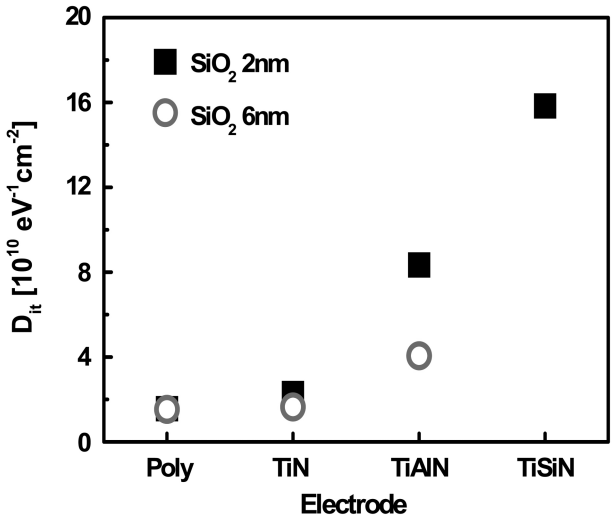

Fig. 14. Electrode dependent D_{it} characteristics. Ternary metal-nitride with a thin SiO_2 sample showed higher D_{it} than thicker SiO_2 and a binary metal-nitride sample.

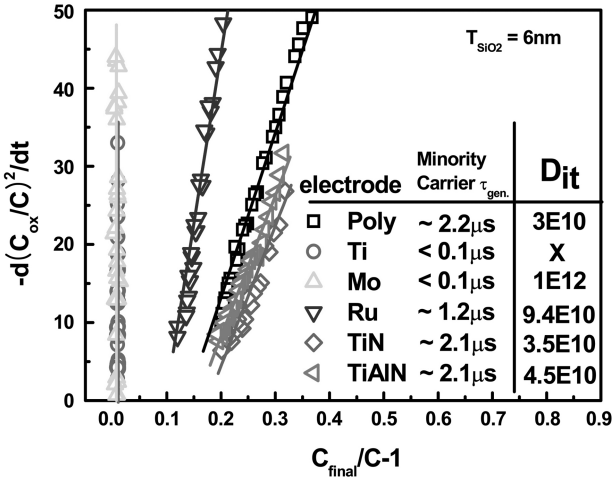

Fig. 15. The Zerbst plot of various electrode capacitors. A fast minority carrier generation time and a significant D_{it} increase were observed in the elemental metal (Ti, Mo) electrode capacitor.

that Ti and Mo atoms have diffused into Si substrate. On the other hand, the TiAlN and Ru electrodes showed long τ_{minor} similar to the polysilicon electrode, but these electrodes the showed degradation of D_{it}, which can be explained by metal atoms diffusion into a dielectric layer only. SIMS analysis of TiAlN and Mo are shown in Fig. 16 and the inset respectively, supporting our observations.

The effects of gate electrode materials on the charge trapping and carrier mobility of metal gate devices are investigated. Binary metal-nitride electrodes showed excellent thermal stability. However, the elemental metal and ternary metal-nitride electrode degraded interface trap density.

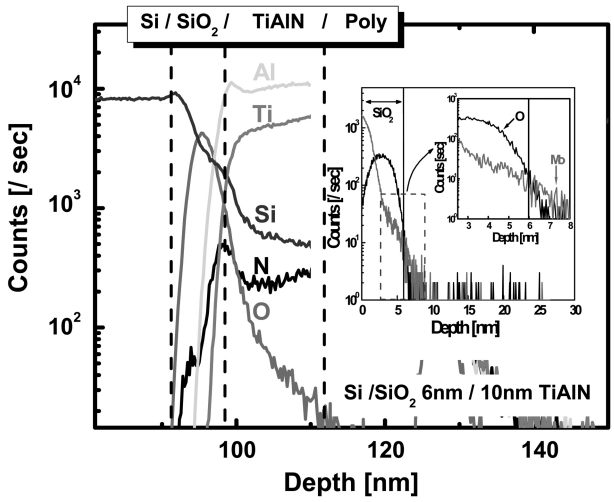

Fig. 16. Backside SIMS measurement of the TiAlN electrode capacitor. Metal diffused to dielectric. The inset figure shows the SIMS data of the Mo electrode capacitor. A clear Mo signal was observed in both the dielectric and substrate.

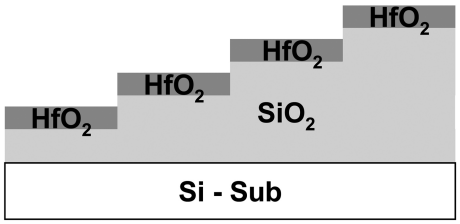

Fig. 17. Schematic diagram of the terraced wafer which was used for these experiments.

2.3.2. Workfunction extraction method with terraced oxide

Usually, the metal gate work function is extracted using C-V analysis. But there are errors involved due to the fixed charge and also errors coming from the EOT and V_{fb} extraction. To extract work function more accurately and neglect the fixed charge variation, a new method has been introduced using terraced (wedding cake type) SiO_2 samples[28]. This gives a varied SiO_2 structure (~6-8 nm) on the same wafer avoiding a different fixed charge effect. A schematic diagram of the sample is shown in Fig. 17. Using this kind of terraced sample, the work function can be calculated using three charge model, including the oxide-silicon interface charge density (Q_f), oxide-high-k interface charge (Q_i) and a bulk high-k film charge density (ρ_b). The SiO_2 bulk charge is few orders of magnitude lower ($Q_{SiO2} \ll Q_{HfO2}$) and can be neglected. Then the equation becomes

$$V_{fb}=\phi_{ms}-Q_i*CETh/\varepsilon_o\varepsilon_{ox}-\rho_b*CETh^2/2*\varepsilon_o\varepsilon_{ox}-Q_f*CET/\varepsilon_o\varepsilon_{ox}$$

where CET=the capacitance equivalent thickness of the gate stack, the sum of CETi, the equivalent thickness of the interfacial oxide (variable in our structure) and CETh, the equivalent thickness of the high-k film (constant in our structure).

Actual values of the second and third terms of this equation are negligible. Considering that the work function can be calculated using a linear fitting of the simple equation shown below

$$V_{fb} = \phi_{ms} - Q_f / \varepsilon_o \varepsilon_{ox} W_{ox}$$

where Φ_{ms} is the work function difference between the metal gate and silicon substrate. Q_f is the fixed charge density, W_{ox} is the EOT of the dielectric stack and ε_{ox} is the SiO_2 dielectric constant (3.9). The thick SiO_2 layer and fixed HfO_2 allow one to neglect the interface charge and enables the use this simple linear equation to extract work function with very small errors.

2.3.3. Sc for NMOS work function

Sc metal is an attractive candidate because of its ultra low work function. However, the Sc metal shows a work function close to its vacuum work function (3.5 eV) on SiO_2 but on high-k oxide like HfO_2, the work function becomes much higher than expected [29]. The workfunction can be improved by preventing reaction between metal gate and high-k dielectric. A thermally stable interface layer can be useful for this purpose. Metallic nitrides like TaN or TiN have been used as a thermally stable diffusion barrier in the silicon back end process. For that reason, a thin TaN layer is used to prevent extensive reactions between Sc and HfO_2.

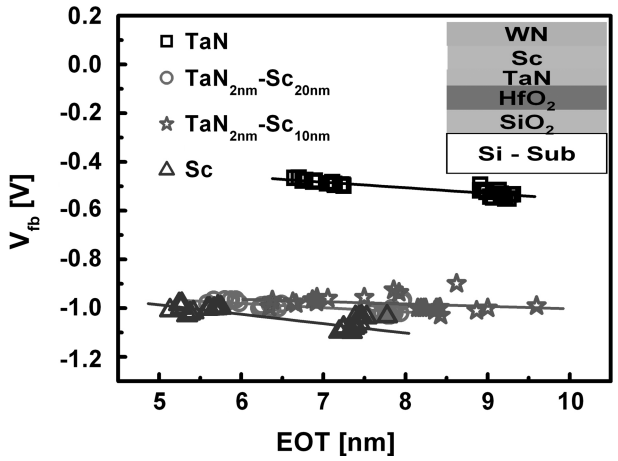

Fig. 18. The V_{fb} vs. EOT data which is used to calculate the work function. The inset figure shows the metal gate stack on terraced gate dielectrics.

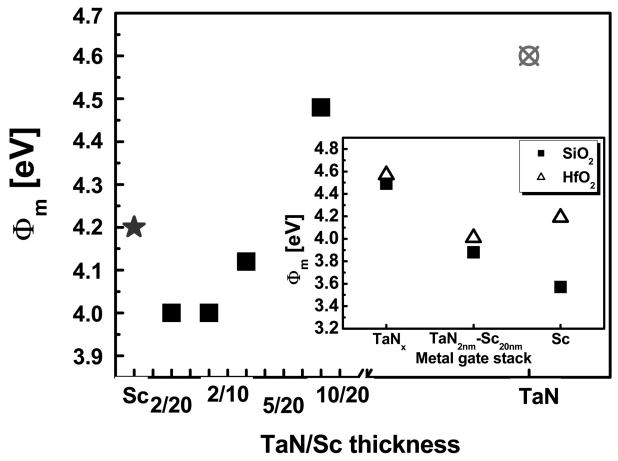

Fig. 19. The work function for different metal gate stack. The inset shows the work function for both SiO_2 (closed) and HfO_2 (Open) gate dielectrics.

Compared with TaN_x gate, the TaN_{2nm}-Sc_{20nm} sample shows significant shift of V_{fb} (Fig. 18). The TaN_{2nm}-Sc_{20nm} sample shows lower fixed charge density compared with the elemental Sc gate. The thickness dependence on workfunction has been evaluated with varying TaN_x and Sc thickness. Figure 19 shows the work function for a different metal gate stack with different TaN_x and Sc thickness. For comparison, a bulk Sc and TaN_x metal gate work function was also shown in the same figure. With a TaN_x thickness of around 2 nm, the work function of 4.0 eV was achieved. The bulk Sc metal gate shows a slightly higher work function of 4.2eV. This is may be due to the interface reaction between Sc metal and high-k gate dielectric materials. With the increasing thickness of TaN_x interface layer to ~10 nm, it shows work function close to bulk TaN_x (~40 nm) metal gate work function of 4.6 eV. The inset of Fig. 19 shows the work function for SiO_2 and HfO_2/SiO_2 samples for different gate electrodes. The TaN_x gate or gate stack with the TaN_x interface layer shows an almost similar work function for both the SiO_2 and HfO_2/SiO_2 gate dielectrics consistent with the previous reports [30]. In contrast, the work function of Sc metal shows a large deviation for SiO_2 and HfO_2/SiO_2 gate dielectrics. The workfunction value of Sc metal on SiO_2 gate dielectric is 3.6 eV, which is close to its vacuum workfunction of 3.5 eV. But for HfO_2/SiO_2, the workfunction increases to 4.2 eV. For covalent SiO_2, the removal of one oxygen atom creates a local Si-Si bond whereas for ionic HfO_2, one oxygen vacancy creates two surplus electrons and causes charge imbalance, which causes the shift in the flatband voltage [24].

2.3.4. Conducting RuO_x as a PMOS metal gate

Some conductive oxides like IrO_2 or RuO_2 are suitable for PMOS metal because conducting oxides might have more resistance to oxygen vacancy formation [31]. Compared with their corresponding elemental metals, these conducting oxides are expected to have a higher work function.

Ru and RuO_x metal was deposited and WF was extracted for RuO_x at varying oxygen amounts with constant Ar pressure. Ru metal has been studied extensively for metal gate application [31-32]. On HfO_2 it shows WF around 5.1-5.2 eV [31]. But RuO_x shows even higher workfunction, depending on the processing conditions [33-34]. Figure 20 shows the C-V characteristics at three different frequencies for both Ru

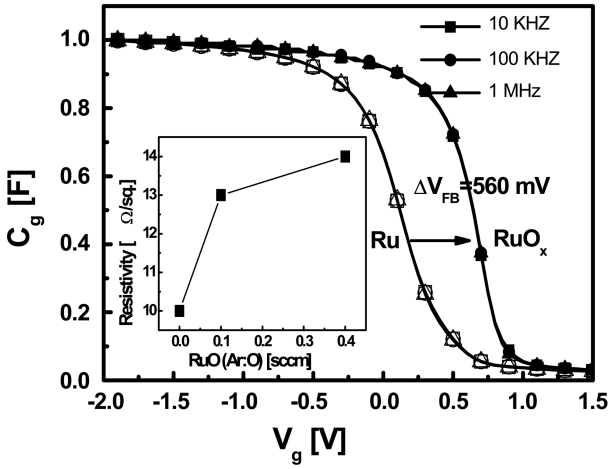

Fig. 20. C-V at different frequencies for Ru and RuO_x (O_2=0.4 sccm) revealing excellent metal-dielectric quality. A C-V flatband shift of 560 mV is observed for RuO_x film. The inset figure shows the sheet resistance for different Ru and RuO_x gate metals.

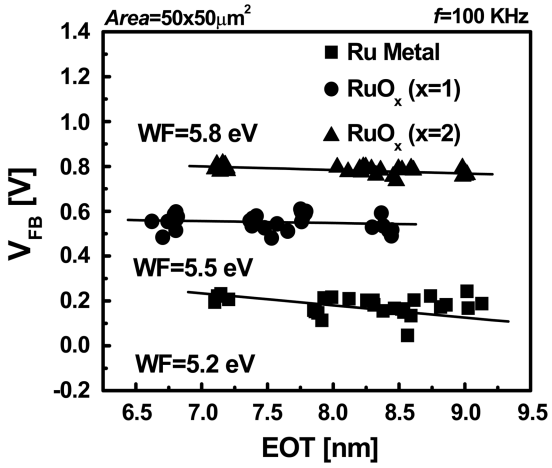

Fig. 21. The work function extraction for different gates. The Ru metal shows work function of 5.2 eV where as it increases with increasing O_2 concentration up to 5.8 eV.

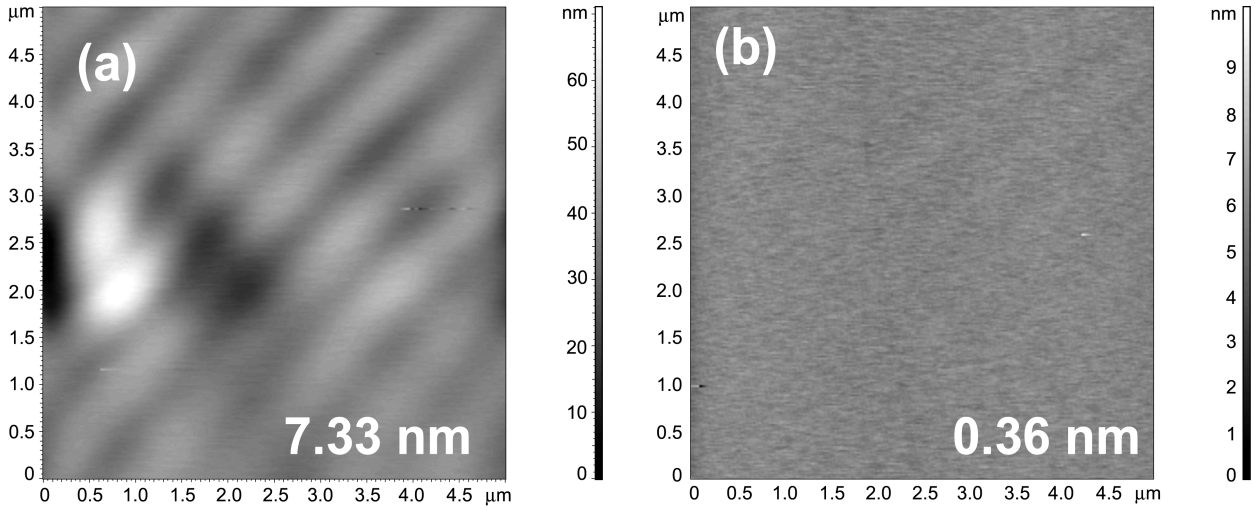

Fig. 22. AFM images of deposited Ru metal (a) and RuO_x (b). Ru metal has very rough texture and the RMS value is over 20 times higher than RuO_x film.

metal and RuO_x metal. No frequency dependency was observed indicating no degradation of dielectric quality. The RuO_x film shows a positive shift of flat band voltage about 560 mV compared with Ru metal gate. The inset figure shows the sheet resistance values for Ru and RuO_x metals. The incorporation of oxygen showed a negligible increase of resistance and can be suitable for metal gate application. Figure 21 shows the EOT versus V_{fb} diagram for work function extraction. By increasing oxygen concentration, V_{FB} tends to increase. A V_{FB} shift as large as 560 mV is observed for high oxygen concentration in comparison with Ru metal. The work function for Ru metal is found to be 5.2eV, close to the already reported data. RuO_x with 0.4 sccm of oxygen, the WF increases up to 5.8 eV. A further increase of O_2 increases the resistivity and also increases EOT considerably, possibly due to additional oxide growth. The increase of WF with increasing O_2 can be attributed to the higher electro-negativity of O_2 as vacuum work function has a relation with electro-negativity as shown below [35]

$$\phi_{vac} = 2.27x_m + 0.34$$

where Φ_{vac} is the vacuum work function and χ_m is the electro-negativity of the metal.

To understand the increase of WF after forming a conductive oxide, we have investigated physical property changes with AFM and XRD analyses. Fig. 22 shows the atomic force microscopy images of Ru and RuO_x film and their RMS values. RuO shows more uniform RMS values than elemental Ru, indicating that RuO can be formed with more

stable and uniform film properties. We have also found that the deposited Ru metal is in the polycrystalline phase, whereas RuO_x is amorphous (XRD data is not shown here). The different work function of polycrystal Ru and amorphous RuO_x can be related to their different phases. As reported, the metal gate work function is also related to the crystal orientation of the metal [36]. Because a different plane has a different electron density and hence different work function.

3. CONCLUSION

In this paper, we have discussed the analyses method and various processes to understand and solve the problems of metal gate and high-k gate dielectrics. These method and process give a better understanding of the nature of high-k gate dielectrics and the higher performance of the CMOS device. By optimizing the process and adopting the analyses, the transistor with a metal gate and high-k gate dielectrics can achieve high performance as well as good reliability.

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