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Crystallization of Amorphous-Silicon by Seed Layer and its Polycrystalline-Silicon Thin Film Transistors

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Recently, it was reported that amorphous silicon (a-Si) thin films could be crystallized at a low temperature (~500°C) using the metal-induced lateral crystallization (MILC) process. The MILC process enables the crystallization of a-Si thin films with less metal contamination. However, some problems remain that need to be solved, such as the complicated process steps and the long annealing time required to crystallize a-Si. In this work, we propose a novel method that simplifies the process and reduces the processing time using a seed layer, which resulted in the crystallization of the a-Si thin film in a shorter time. We also fabricated poly-Si TFTs to confirm the quality of the poly-Si that was crystallized by the novel method. The poly-Si TFTs using the Ni seed layer, which exhibited a filed effect mobility of 42.1cm^2/Vs and an on/off ratio of 1.9×10^6 V/dec; these values are similar to those of the poly-Si TFTs fabricated using the conventional MILC process.

Keywords: MILC, seed layer, Ni silicide, poly-Si TFTs

1. INTRODUCTION

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) are a very attractive technology for application in active matrix displays with built-in drivers fabricated on glass substrates. The most widely employed methods for poly-Si formation are furnace annealing for solid-phase crystallization (SPC)[1] and eximer laser annealing (ELA).[2] SPC is a well known process, but the normal crystallization temperature, which is near 600°C, is very high for common glass substrates. ELA methods were developed in order to achieve high performance in the TFTs, but many problems remain to be resolved.[3] However, it has been reported that the crystallization annealing temperature of a-Si thin film could be lowered below 500°C by the addition of some metals.[4-5] However, despite the low thermal budget, the poly-Si thin films crystallized by metal induced crystallization (MIC) have serious problems when applied to poly-Si TFTs due to the metal contamination in the channel layers. Metal contamination in the channel layer can degrade the field effect mobility and anonymous leakage current.[6]

Recently, a metal-induced lateral crystallization (MILC) process has been introduced where amorphous silicon (a-Si) thin films were crystallized at a low temperature of below 500°C.[7-8] It was reported that high performance poly-Si TFTs could be successfully fabricated through Ni-MILC.[7, 9, 10] However, some problems remain that need to be solved, such as the complicated process steps and the long annealing time required to crystallize a-Si.

In this work, we propose a novel method to simplify the process and reduce the processing time using a Ni seed layer. We could crystallize the a-Si thin film in a shorter time than that of a-Si via MILC using a Ni seed layer. We also fabricated poly-Si TFTs to confirm the quality of the poly-Si that was crystallized using the novel method.

2. EXPERIMENTAL DETAILS

To observe the growth aspects of poly-Si crystallized using a Ni seed layer, a 3000 Å thick SiO_2 layer was deposited on a glass substrate as a buffer layer via plasma-enhanced CVD (PECVD) using SiH_4 and N_2O gas at 420°C, and then a 600 Å thick a-Si thin film (first a-Si layer) was deposited on the glass (Corning 1737) substrate via a low-pressure chemical vapor deposition (LPCVD) using disilane (Si_2H_6) gas at 550°C. A Ni film of 50 Å thickness was deposited via direct-current magnetron sputtering at room temperature. The a-Si below Ni was crystallized by rapid thermal annealing at 300°C in a vacuum for 1 h, and the remaining Ni was removed by $HNO_3 + HCl + H_2O_2$ etchant. This is called the Ni seed layer. Next, a 600 Å thick a-Si thin

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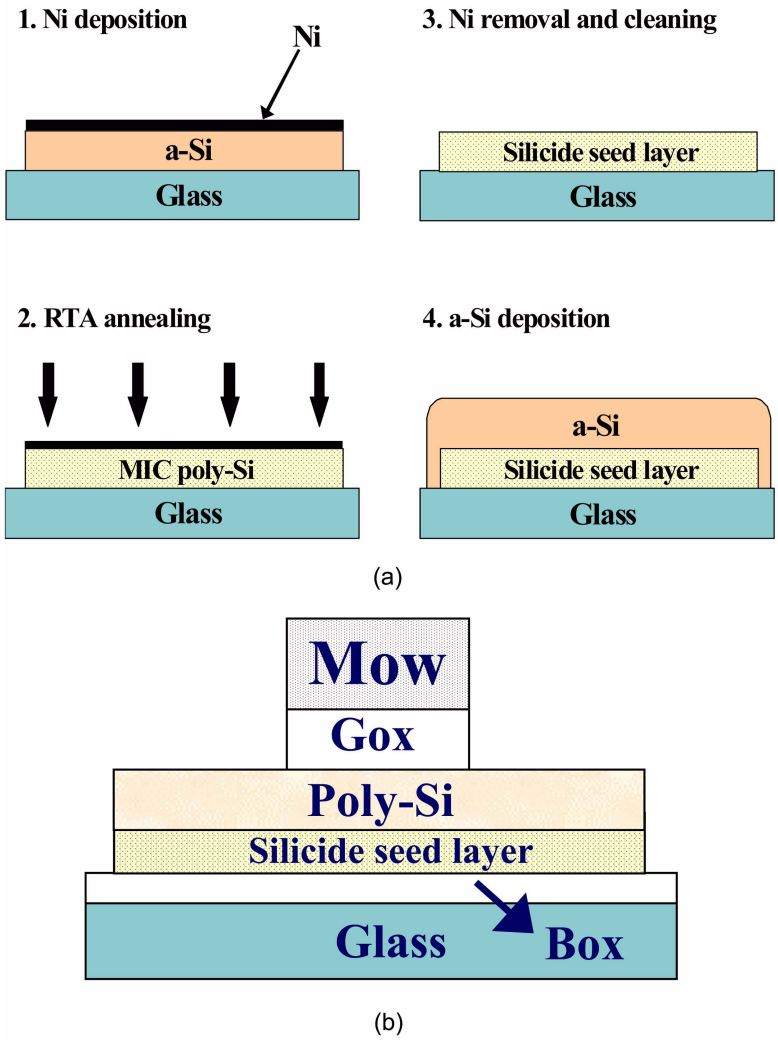

Fig. 1. (a) Process steps of crystallization using a seed layer, and (b) schematic diagram of the fabricated seed layer TFT.

film (second a-Si layer) was deposited on the Ni seed layer/glass substrate via LPCVD using disilane (Si_2H_6) gas at 550°C. The process steps of the Ni seed layer are shown in Fig. 1(a). The samples were annealed at 550°C in a vacuum for 1 h to crystallize the second a-Si layer through the first a-Si layer.

To investigate the quality of the Ni-seed MILC poly-Si, p-channel MILC TFTs were fabricated. The channel dimensions of the p-channel TFTs were 10 µm wide and 10 µm long. An active layer was patterned, and then a 1000 Å thick gate oxide was deposited via plasma-enhanced CVD (PECVD) using SiH_4 and N_2O gas at 420°C. Next, an MoW gate metal with a thickness of 2000 Å was formed by sputtering. The gate metal was etched using $H_3PO_4 + CH_3COOH + HNO_3 + H_2O$ etchant, and the gate oxide was etched via RIE using SF_6, Ar, and CHF_3 gas. The source-drain region was doped through an ion mass doping system using a B_2H_6 source gas. The accelerating voltage and radio frequency power were 15 keV and 150 W, respectively. The samples were annealed at 570°C for 2 h in H_2 ambient to crystallize the a-Si and dopant activation. The electrical properties of the TFTs were measured using HP4140B.

3. RESULTS AND DISCUSSION

In the conventional MILC process, Ni seeds are formed only in the desired areas on the a-Si film by MIC, and then the a-Si film is crystallized laterally [9, 10] and a channel region can be crystallized. In the proposed process, however, Ni is deposited on the first a-Si layer to form a Ni seed layer, and then the second a-Si layer is crystallized by the first a-Si layer (seed layer). As shown in Fig. 1(a), when a Ni film of 50 Å thickness was deposited on the first a-Si layer, annealed for MIC, and then the second a-Si layer was deposited after Ni removal, Ni seeds were formed on the second a-Si layer using the Ni silicide on the first a-Si layer as shown

Fig. 2. Figure 2 shows that there are many nuclei inside the Ni seed layer, and one nucleus consisting of Ni silicide is in one crystal. Figure 3 shows the crystallization stages of the MIC region crystallized via the Ni seed layer as the annealing time increases. Annealing was performed at 550°C in a vacuum. As Fig. 3(a) shows, the a-Si deposited on the Ni seed layer was crystallized by the Ni silicides first and then grew gradually as the time increased. Finally, the MIC region was fully crystallized, and lateral growth occurred as shown Fig. 3(d). Figure 4 shows the MIC region crystallized using the Ni seed layer after chemical etching with a secco etchant. The secco etchant can etch a-Si and Ni silicide selectively. As Fig. 4 shows, there are many nuclei inside the Ni seed layer. The crystallization proceeds from these nuclei, meets neighboring grains, and finally forms a grain boundary. These results show that the crystallization resulting from the Ni seed layer is distinctly different from that which results from using Ni metal. Therefore, it was found the Ni seeds consist of only Ni silicides and the lateral growth was due to only the Ni silicides that were in the Ni seeds. The crystal dimensions crystallized by the seed layer were approximately 10~20 μm. The microstructures of the MIC (Ni seed layer)/MILC boundary with FESEM after the secco

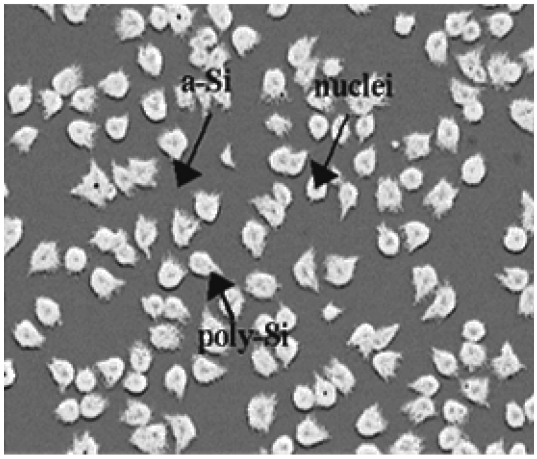

Fig. 2. Optical microscope images of the front silicon region crystallized via the seed layer before annealing.

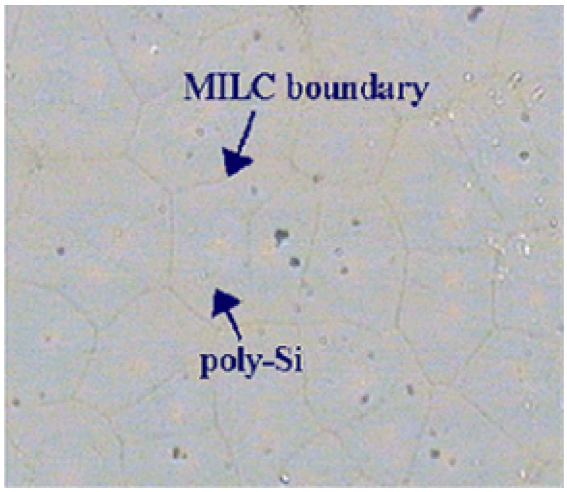

Fig. 4. Optical microscope images of the front silicon region crystallized using the seed layer after annealing (secco etching).

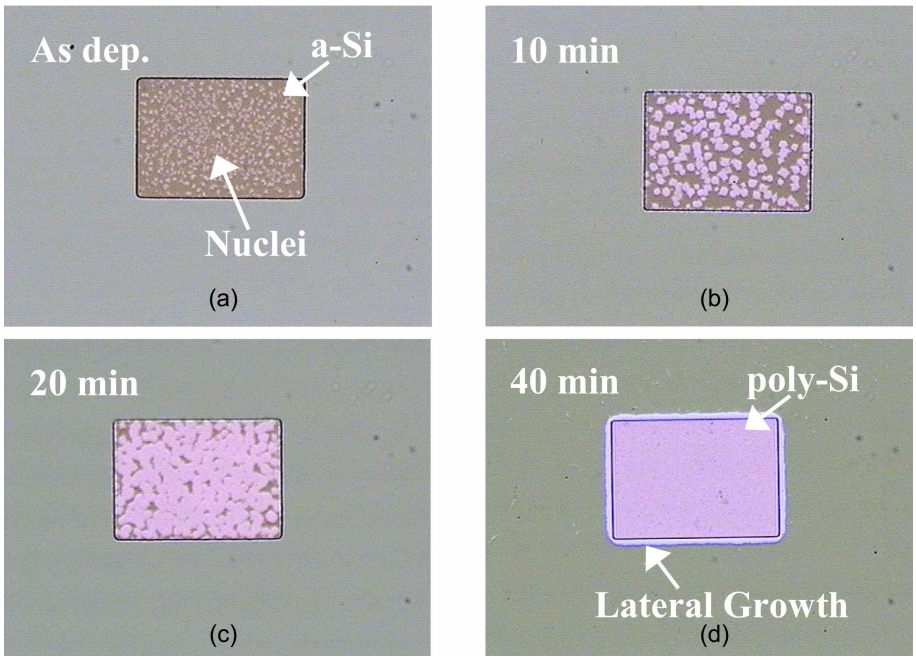

Fig. 3. Crystallization stages of MILC caused by the Ni seed: (a) after the second a-Si deposition, (b) after 10 min, (c) after 20 min, and (d) after 40 min of thermal annealing by RTA.

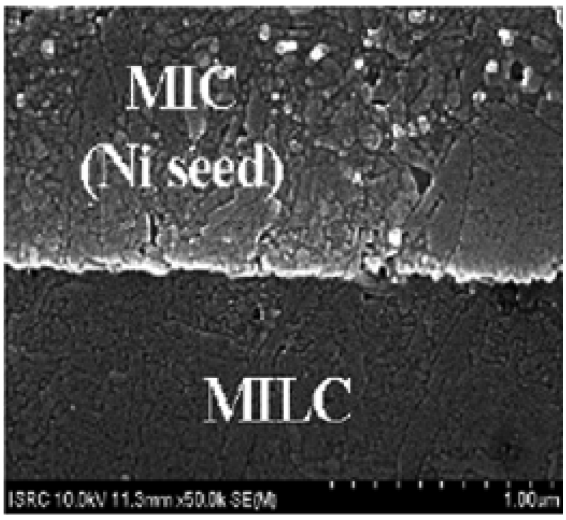

Fig. 5. FESEM image of MIC (Ni seed) and MILC boundary crystallized using the Ni seed.

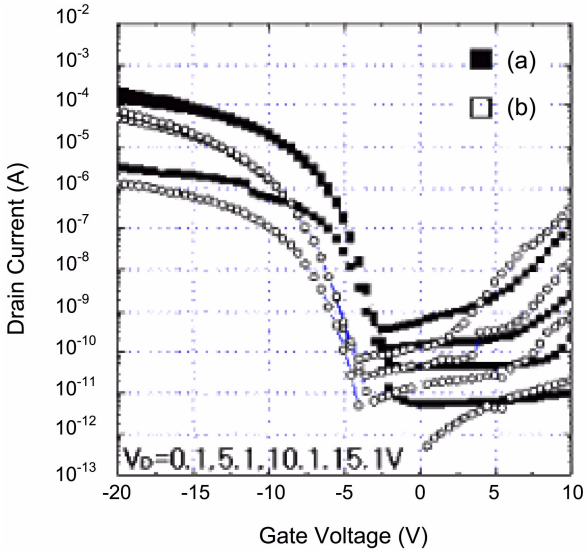

Fig. 6. The electrical properties of the p-type poly-Si TFTs that were fabricated via the (a) MILC process and (b) seed layer.

etching are shown in Fig. 5. The figure shows that not only the MILC region but also the MIC (Ni seed layer) region has good quality poly-Si, which means there are no void or small grain boundaries in the poly-Si. That is, the poly-Si crystallized using the Ni seed layer has a large grain size and good quality.

Figure 6 illustrates the electrical properties of the p-channel poly-Si TFTs that were fabricated using the conventional MILC process and the Ni seed layer. The closed symbol represents the current-voltage characteristics of the conventional MILC poly-Si TFTs, while the open symbol represents that of the seed layer poly-Si TFTs. The minimum leakage current of the p-channel seed layer TFTs decreased from 0.25 to 1.24×10^{-11}. Also, the seed layer TFTs had a higher on/off ratio than the conventional MILC TFTs. However, the on current of the p-channel seed layer TFTs decreased from 7.82 to 0.19×10^{-5} A and the field-effect mobility decreased from 62.4 to 42.1cm^2/Vs. That is, the electrical performances in the seed layer TFTs compared with the conventional MILC TFTs were almost identical. This phenomenon was systematically observed for all TFTs with different channel dimensions. Among the channel dimensions, the detailed device parameters of the p-type TFTs with a 10 μm width and a 10 μm length are summarized in Table 1. These results can explain the good electrical properties of the seed layer TFTs. Furthermore, in contrast to the process of the conventional MILC TFTs, the process of the seed layer TFTs used a much shorter annealing time to crystallize the a-Si. Also, there was no mask step needed to form the Ni seed layer and crystallize the a-Si. Thus, the overall processing time could be reduced.

4. SUMMARY

In summary, we proposed a novel method to simplify the process and reduce the processing time required to crystallize a-Si using a seed layer. In contrast to the conventional MILC TFT process, the proposed process using seed layer TFTs required a shorter annealing time to crystallize a-Si,

Table 1. Detailed device parameters of the MILC poly-Si TFT and the seed layer poly-Si TFTs (W/L=10:10 μm)[a]

Parameters	MILC TFTs	Seed layer TFTs
Subthreshold slope (V/dec}	0.70	0.69
Threshold voltage (v)	-6.0	-9.1
Field-effect mobility (cm^2/Vs)	62.4	42.1
Minimum leakage current ($\times10^{-10}$ A)	0.25	1.24
On current ($\times10^{-5}$A)	7.82	0.19
Maximum on/off ratio ($\times10^{-6}$ A)	2.63	1.57

[a] The threshold voltage was defined at a normalized drain current ($I_{DS}\times W/L$) of 1 μA at V_D = 10.1 V. The subthreshold slope was defined as the voltage required, increasing the drain current by a factor of 10, and the field-effect mobility was calculated in the linear region at V_D = 10.1 V. The maximum on/off ratio was determined at V_D = 10.1 V and V_G = -20 – 10 V.

and there was no mask step to form the Ni seed layer and crystallize the a-Si. Therefore, we could reduce the overall processing time. We also fabricated poly-Si TFTs to confirm the quality of the poly-Si that was crystallized using the novel method. Compared with the conventional MILC TFTs, the electrical performances in the seed layer TFTs were almost identical. From these results, we concluded that good quality poly-Si TFTs can be fabricated in a shorter time using the seed layer.

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