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Resistive Switching Properties of Pt/TiO_2/n^+-Si ReRAM for Nonvolatile Memory Application

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We fabricated sputter-Pt/atomic layer deposition (ALD) TiO_2/n^+-Si structures for resistive random access memory (ReRAM). The use of n^+-Si bottom electrode provides a simple way of fabricating ReRAMs, and offers compatibility with the conventional CMOS process. After annealing Pt (100 nm)/ ALD TiO_2(38 nm)/ n^+-Si structures in an O_2 ambient at a temperature range of 100 to 500°C, we examined their effects on the switching properties. The as-deposited ALD TiO_2 thin films showed no switching behavior. However, annealing at 100°C enabled the thin films to switch between a low- resistance state and a high-resistance state, thereby revealing the resistive switching behavior. In addition, electric pulse-induced resistance switching was repeated (about twenty times) in the 100°C-annealed TiO_2 films. When the annealing temperature was increased to 300°C, the switching properties of the TiO_2 thin films were significantly improved in terms of the resistive switching cycle and the dispersion of the set/reset voltages, probably due to the improved crystallization of the TiO_2 films and the enhanced anode interface properties. As a result, the simple structure of Pt/ALD TiO_2/n^+-Si can be applied to nonvolatile memory devices.

Keywords: TiO_2, resistive switching, memory effects

1. INTRODUCTION

Resistive switching in TiO_2 thin films has attracted significant attention for possible application in nonvolatile semiconductor memory devices.[1-3] This potential exists because a resistive random access memory (ReRAM) consisting of a simple metal-insulator-metal structure has the advantages of low power consumption, high-speed operation, and high density integration.[4-7] However, although the switching behavior can be clearly observed and possible models involving the band bending theory and the filament current have been suggested, the nature of the switching mechanism is still unclear.[8-11] This lack of understanding is partly due to the poorly defined quality of the resistive switching materials in the literature. In addition, the thickness of resistive switching materials needs to be down-scaled to less than a few hundred nanometers to enable the devise to operate at a low voltage (<1 V), which is essential for mobile applications. More importantly, because the resistive switching behavior depends strongly on the thickness, the thickness must be kept uniform for its proper application in devices.[12] Atomic layer deposition (ALD) has the ability to provide nanoscale thickness control, hence it offers excellent thickness uniformity, though the quality of ALD thin films varies due to a low thermal budget.

On account of its advantages, we used the ALD method to deposit a uniform thick layer of TiO_2 thin film on an n^+-Si substrate; we then sputtered Pt on the layer. This process yielded a Pt/TiO_2/n^+-Si structure, which we then annealed in an O_2 ambient to examine how the film quality, especially in terms of crystallization, affected the switching performances (namely the dispersion of memory switching parameters such as the set/reset voltage and the high/low resistance state, as well as the number of switching cycles).

2. EXPERIMENTAL

A highly doped n-type Si(100) was used as a bottom electrode. We then deposited a 38 nm thick layer of TiO_2 thin film on the highly doped n-type Si(100) by using the ALD method in a cold-wall reactor at 130°C. Next, we used $Ti(OCH(CH_3)_2)_4$ (TTIP) as a Ti precursor and H_2O as an oxidant. One deposition cycle consisted of a 2 s pulse of the Ti precursor, a 30 s purge of Ar, a 2 s pulse of H_2O, and a 60 s purge of Ar. We then used 5 sccm of N_2 was used as a carrier gas to deliver the Ti precursor and 200 sccm of Ar as a purge gas, while maintaining the processing pressure at 800mTorr. The growth rate of TiO_2 per cycle was 0.38 Å. The bubbler for the TIPP, which has an equilibrium pressure of 0.1 Torr at 49°C,[13] was maintained at 32°C and the gas delivery line was maintained at 42°C to prevent condensation of the Ti

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precursor. The post annealing of the ReRAM device was performed at a temperature range of 100°C to 500°C for 30 min in an O_2 ambient. We subsequently deposited a 100 nm thick Pt top electrode by means of magnetron sputtering over a photoresist prepatterned TiO_2 surface and then used acetone to remove the patterned photoresist with Pt. This process yielded Pt films patterned with 80 μm diameter dots.

We used an ellipsometer to measure the thickness of the deposited TiO_2 thin film. The structural properties of the TiO_2 thin film were then characterized with the aid of X-ray diffraction (XRD). Next we used Auger electron spectrometry (AES) to identify the film impurities such as Pt, Ti, Si, O in the films and to determine the diffusion of Pt and Si in the TiO_2 layer. Finally, the resistance switching properties were measured with a semiconductor parameter analyzer (Agilent 4145A).

3. RESULTS AND DISCUSSION

Figure 1 shows XRD spectra of the as-deposited Pt/TiO_2/n^+-Si structures and the as-annealed structures. The as-deposited ALD TiO_2 thin film, which is amorphous, becomes an anatase structure after being annealed at 100°C for 30 min. As the post-annealing temperature increases, the crystallinity of the film tends to improve.

Figure 2 shows the current - versus - voltage (I-V) characteristics of the as-deposited Pt/TiO_2/n^+-Si structures and the as-annealed structures at a temperature range of 100°C to 500°C. A positive bias was applied to the top Pt electrode while the bottom electrode was grounded. Figure 2 (a), which shows the initial off state I-V curve of the as-deposited films, reveals that no resistance switching occurred in the films. As with the leakage current, the resistance characteristics indicate that the as-deposited TiO_2 thin films have

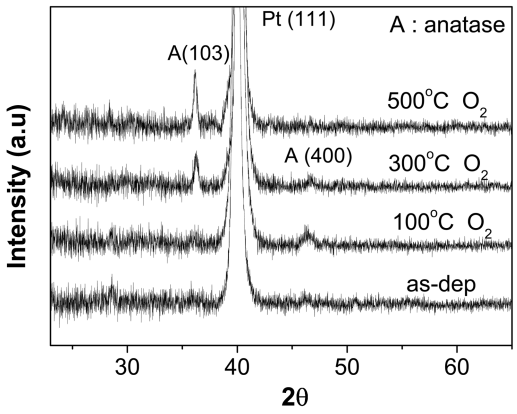

Fig. 1. XRD spectra of multiple Pt/ TiO_2/n^+ Si layers post-annealed at various temperatures.

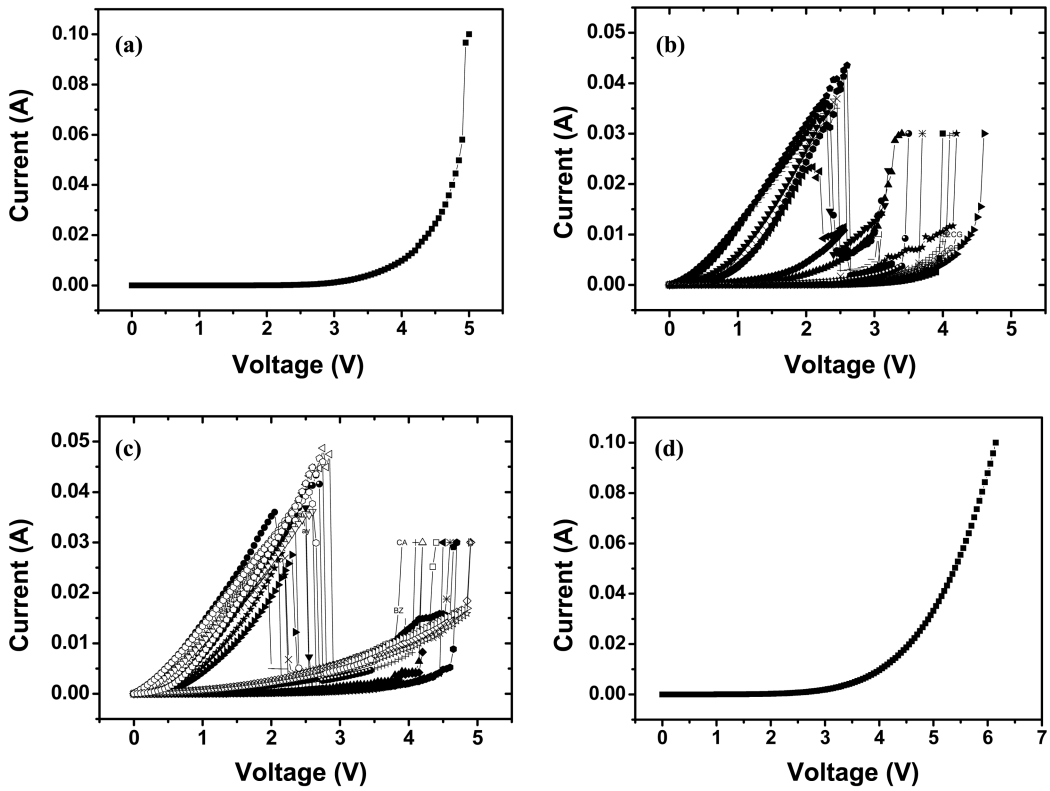

Fig. 2. An I-V curve of post-annealing dependence of memory switching in Pt/TiO_2/n^+ Si (100) for post annealing at (a) room temperature, (b) 100°C, (c) 300°C, and (d) 500°C.

amorphous structures that provide defects and these defects act as current paths for leakages rather than a filament current flow. We deduce that the filament current flows through the inside of the grains instead of along the grain boundaries. Note also, as shown in Fig. 2(b), that even when a sample is annealed at 100°C the resistance switching characteristics can be observed. We measured these characteristics with a current compliance of 30 mA after electroforming with a positive voltage on the top electrode. As shown in Fig. 2(c), the repetitive switching between a high resistance state (HRS) and a low resistance state (LRS) continues until approximately 20 cycles of switching. The set switching takes place in a range of 3.0 V to 4.3 V and the reset switching in a range of 2.3 V to 2.5V. In addition, Fig. 3(a) and 3(b) show that the HRS and the LRS are both stable at a read-out voltage of 0.1 V, at which the resistance ratio of the HRS to the LRS is 15−1000; these figures also show that when the annealing temperature is increased to 300°C significantly improves the resistive switching performances in terms of the dispersion of high and low resistance, the difference between set and reset voltages, and the number of switching cycles. Note also that when the Pt/TiO_2/n^+-Si sample is annealed at 300°C the number of switching cycles is increased remarkably to approximately 100, and there is a greater difference between set and reset voltages. As a result, the ReRAM performance is more reliable. However, due to the relatively high resistance in the set on-state at the lower voltage, the resistance ratio of the HRS to the LRS is about 100 at a read-out voltage of 0.1 V. When the post-annealing temperature is raised to 500°C, the resistive switching of Pt/TiO_2/ n^+-Si disappears, as shown in Fig. 2(d), even though the crystallinity of TiO_2 thin film is highly improved.

Figure 3 compares the I-V characteristics in the low resistance set state of Pt/TiO_2/n^+-Si structures with those of Pt/TiO_2/Pt samples. This comparison enables us to examine how the bottom electrode affects the electrical resistance of the ReRAM device. The resistance of Pt/TiO_2/n^+-Si is much higher than that of Pt/TiO_2/Pt, especially at the low applied voltage. The inset of Fig. 4 shows the log(I)-log(V) curves in the low resistance set state at a low applied voltage (< 0.5 V). Note that the measured slopes of the log(I)-log(V) curves in the inset of Fig. 4 are approximately 0.97 for Pt/TiO_2/Pt and 1.0 for Pt/TiO_2/n^+-Si.

Because the current density-voltage (J-V) equation in the Ohmic conduction is

$$J = qn_0\mu_n\frac{V}{d_s} \quad (1)$$

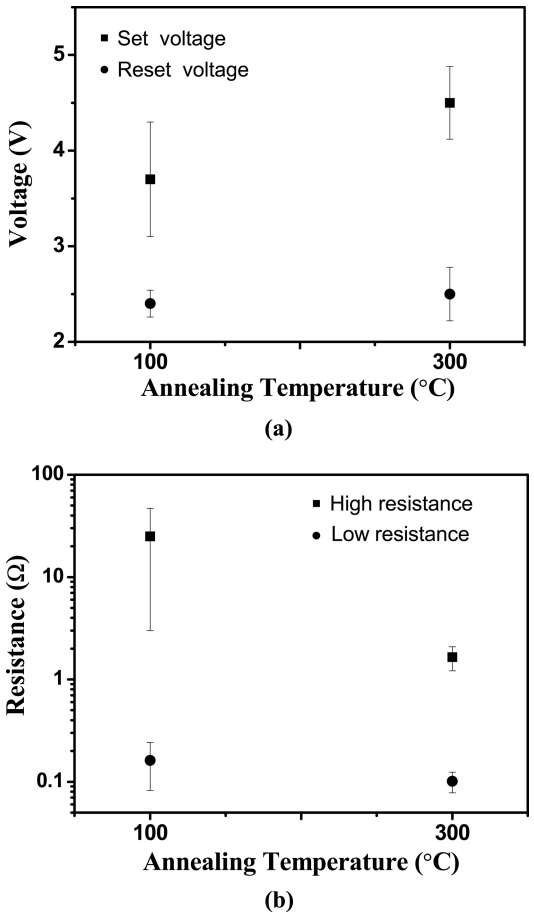

Fig. 3. (a) The set/reset voltages and (b) high/low resistance in TiO_2 films as a function of the post- annealing temperature. The high/low resistances were measured at V=0.1 V in each memory state.

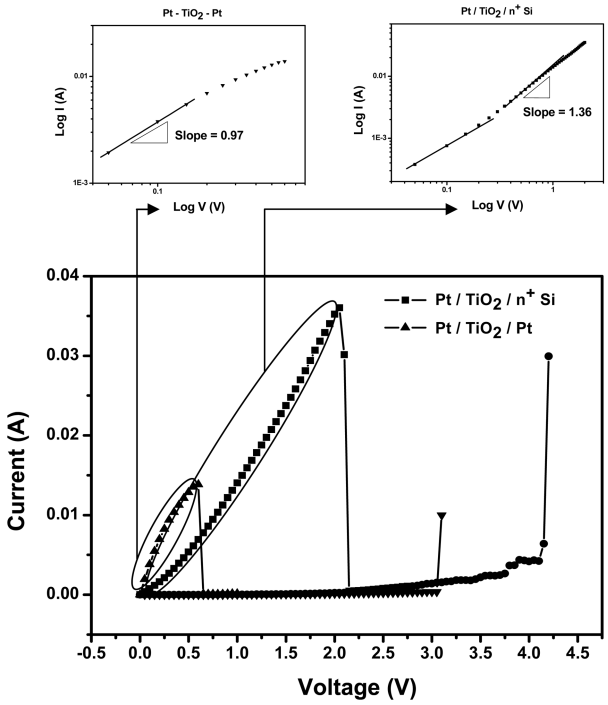

Fig. 4. A plot of the log(I) vs. log(V) curves in the low resistance set state of Pt/TiO_2/n^+ Si device and a Pt/TiO_2/Pt device at a low applied voltage.

where q is the elementary charge, ì$_n$ is electron mobility and d_s are the thickness of an actual switching layer in the TiO_2 film.

The J-V equation for the space charge limited conduction is as follows

$$J = \frac{9}{8}\varepsilon\mu_n\theta\frac{V^2}{d_s^3} \quad (2)$$

where is the dielectric constant.[14] On the basis of Eqs. (1) and (2), we deduce that the conduction of Pt/TiO_2/Pt follows Ohm's law, whereas the conduction of Pt/TiO_2/n^+-Si most likely follows Ohm's law at a very low voltage and then switches to a different mechanism, such as a space charge limitation. This mechanism may be partly due to a lower work function (4.1 eV to 4.2 eV) of n^+-Si than that of Pt (5.6 eV) and partly due to the creation of a high trap density at the interface of TiO_2 and n^+-Si. However, further study is needed to explore the mechanism in detail.

In addition, AES analysis was conducted to determine how much Pt and Si diffused into the TiO_2 thin film during annealing at 500°C. Figure 5 shows the AES depth profiles of the as-fabricated Pt/TiO_2/n^+-Si structure and the structure of the sample annealed at 500°C. The annealing at 500°C enables the Pt to be diffused into the TiO_2 thin film and to come in contact with the Si that is diffused from the n^+-Si substrate. This phenomena probably leads to an electrical short-circuit and a loss of resistive switching behavior.

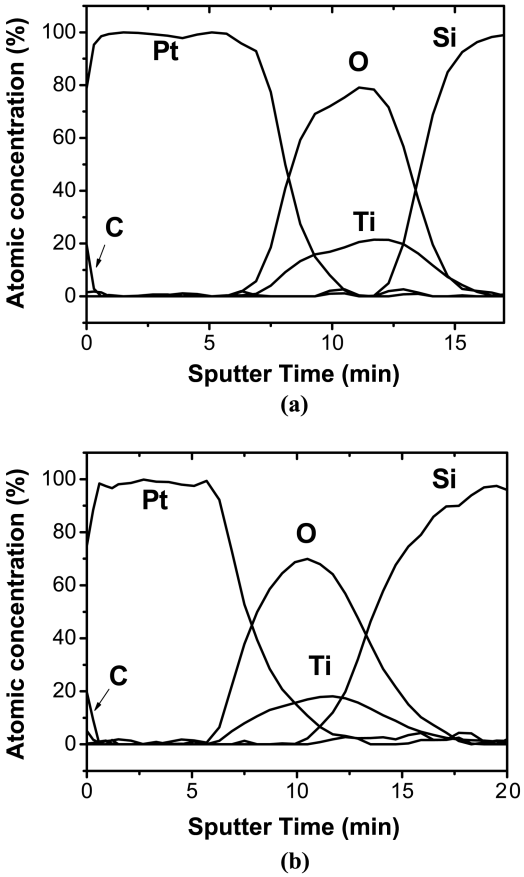

Fig. 5. AES depth profile of (a) as-deposited and (b) post-annealed TiO_2 film at 500°C.

4. CONCLUSIONS

We used highly doped n-type Si (100) as a bottom electrode to fabricate a simple ReRAM structure consisting of Pt/ALD-TiO_2/n^+-Si structures. However, due to the amorphous phase of the as-deposited ALD TiO_2 thin films, the as-fabricated Pt/ALD-TiO_2/n^+-Si did not show any resistive switching behavior. The post-annealing in an O_2 ambient transforms the amorphous TiO_2 thin film into an anatase phase, thereby enabling the resistive switching behavior of the as-annealed TiO_2 thin film. When Pt/TiO_2/n^+-Si is annealed at 300°C the resistive switching performance is more reliable: that is, it has more than 100 resistive switching cycles, a narrow dispersion of high and low resistance, and a large difference between set and reset voltages. As a result, this simple ReRAM structure with an n^+-Si as a bottom electrode can be used as a future nonvolatile memory device.

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