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A Noble Fabrication Method for High Performance Low Temperature Poly Silicon TFT by MILC

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High leakage current and relatively low electron mobility are regarded as obstacles for industrialization of MILC TFT, and many studies have focused on finding solutions to these problems. It is known that MILC induces volume shrinkage and, in a normal process, considerable stress is expected to be built up at the interface between the gate oxide and the substrate silicon during MILC annealing. In this work, the gate has been formed after lateral crystallization of a-Si in order to eliminate the stress effect on the TFT performance. As a result, the leakage current is lowered to 30~40 pA, as compared to a typical level of roughly 100 pA, and an electron mobility of 50~60 cm^2/V Sec can be obtained, as opposed to the general case of around 20~30 cm^2/V Sec.

Keywords: MILC, LTPS, stress, leakage current

1. INTRODUCTION

The characteristics of a flat panel display device, such as brightness, resolution, and image transport speed, are strongly dependent on the electron mobility of TFTs, which in turn depends on the crystallinity of the silicon thin film substrate. Accordingly, many studies have focused on the development of low temperature poly crystallization techniques[1]. In particular, most advanced devices such as DMB (Digital Multimedia Broadcasting) and AMOLED (Active Matrix Organic Light Emitting Display) require poly TFT. As such, the demand for poly TFT in the market is expected to grow exponentially[2-3]. To date, ELS (Excimer Laser Scanning) is the sole technology for LTPS (Low Temperature Poly Silicon). However, it suffers from two major problems in terms of industrialization: 1) the inevitable scan overlap results in non-uniform crystal quality, and 2) the surface roughness caused by the liquid-solid phase transformation requires chemo-mechanical polishing, which is not a trivial process at an industrial level[4-6]. Solutions to these problems have yet to be reported in the literature.

MILC (Metal Induced Lateral Crystallization) technology, which involves a batch process and a solid-state phase transformation, is a relatively lesser known technology compared to ELS. However, MILC does not require additional expensive process equipment such as a laser and is therefore regarded as a viable alternative for the laser process[7-11]. Currently, much work has focused on the development of technologies related to the reduction of leakage current and enhancement of electron mobility in MILC TFTs. In this work, a series of new fabrication processes has been developed in an effort to reduce leakage current in MILC-TFTs. The processes introduced in this work are basically motivated from the attribute that considerable volume change occurs as the MILC induces stress at the gate, which is related to the electrical performance of TFT.

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2. EXPERIMENTAL

Four-inch Corning 1737 glass was used as a substrate. A 3000 Å buffer-oxide was formed on the glass substrate by PECVD, and a 600 Å a-Si thin film was deposited by LPCVD. The active area was then defined. A contact mask was used in order to define Ni on the active area, as shown in Fig. 1, and the substrate was annealed at 600 °C for 2 hours in a hydrogen ambient after nickel deposition followed by a lift-off process. The gate oxide was then deposited by PECVD and the gate, MoW, was deposited by sputtering. The thicknesses of the gate oxide and the gate were 700 Å and 2000 Å, respectively. The gate was formed after the MILC process, in contrast from the conventional process where MILC process is carried out after formation of the gate. Figure 2 shows the formation of the gate after MILC, where the source and drain areas as well as the channel of TFT have already been crystallized. Afterwards, the source

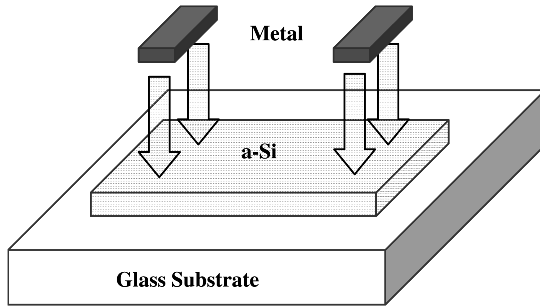

Fig. 1. Formation of Ni catalyst on the areas for S/D.

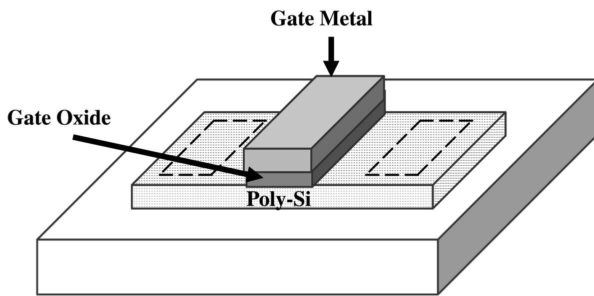

Fig. 2. Formation of the gate after MILC. Ni deposited on S/D is indicated as a dotted line.

and drain were formed with an ion mass doping system. Heat treatment at 550 °C was conducted for one hour for electrical activation. Other processes were carried out in accordance with the typical processes employed for TFT fabrication in a class 100 environment. Each fabricated PMOS TFT was finally analyzed at a 4-point probe station.

It should be noted that the gate is formed after completion of crystallization by MILC.

3. RESULTS AND DISCUSSION

In Fig. 3, the I-V curves of the P-TFT fabricated in this work are shown and the electrical parameters are summarized in Table 1. The length and width are both 10 microns. The electrical parameters in Table 1 are the values at the drain voltage of 10 volts. It should be noticed that the mobility and leakage current are sufficient for practical use. The critical feature in the fabrication processes is that the gate was formed after crystallization and hence stress that might be induced by the volume change during MILC can be avoided. Another important aspect is the electrical activation of the source and drain. In this process, the source and drain were crystallized first and then IMD was carried out. Therefore, before the electrical test, the source and drain had to be heat-treated at 550 °C in hydrogen ambient for one hour for electrical activation. In the conventional process, MILC is typically carried out after IMD on the source and drain and thus extra heat treatment after MILC is not needed for the electrical activation.

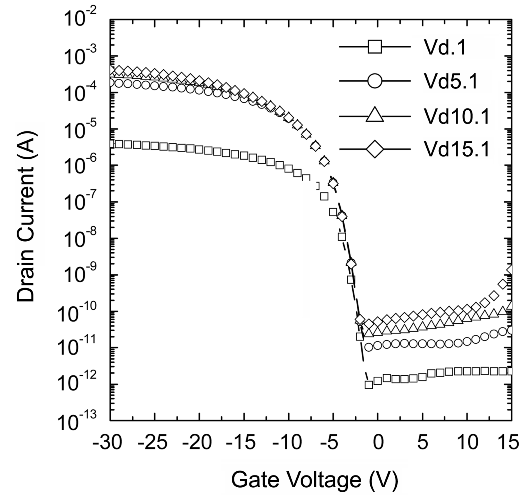

Fig. 3. I-V curves of P-TFT with fabrication sequence of MILC +gatation+IMD.

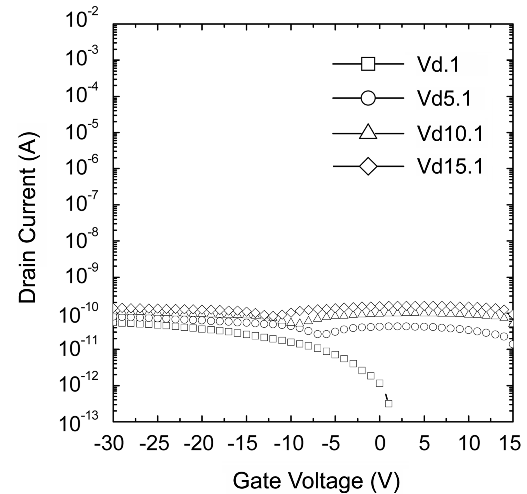

Fig. 4. I-V curves of P-TFT without the electrical activation. Other process conditions correspond with those in Fig. 3 except the electrical activation.

Figure 4 shows the I-V curves of P-TFT corresponding with those in Fig. 3 but without electrical activation just before the measurement. It can be seen that the electrical activation is essential to obtain good results with the pro-

Table 1. Electrical parameters of Fig. 3.

	Vth	Swing	Mobility	On Current	Off Current	On/Off
10×10	-5.5	0.62	54.52	$3.19*10^{-4}$	$3.64*10^{-11}$	$1.39*10^{7}$

posed MILC TFT. It was found that the sheet resistance of the source and drain was around 500 Ω/s after electrical activation. The sheet resistance was more than 1,000 Ω/s before electrical activation. Interestingly, a temperature of 550 °C is adequate for electrical activation in P-TFT when boron is implanted by IMD. In VLSI, where higher implantation energy than IMD is used for the source and drain, a temperature of around 950 °C is typically used for the electrical activation.

In Fig. 5, the I-V curves of P-TFT with the conventional fabrication processes are shown and the electrical parameters are summarized in Table 2.

Comparing the parameters in Table 2 with those in Table 1, high leakage current a considerable reduction in the electron mobility should be noted for this case. Volume shrinkage with crystallization by MILC can be identified with AFM, as shown in Fig. 6; however, the degree of shrinkage has not been measured. If MILC is carried out after gate formation, stress induced by this volume shrinkage should be built up at the channel area of the P-TFT. This stress could be responsible for the low electron mobility and high leakage current.

Higher threshold voltage is observed in the P-TFT fabricated via the conventional process as compared to that developed by the new process, as shown in Fig. 3. The higher threshold voltage might be related to the tensile stress at the interface between the gate oxide and poly silicon at the channel. It is known that interface trapped charges located at the silicon side are usually negative, and tensile stress may promote the formation of these negative charges at the silicon side of the interface. The threshold voltage should compensate these extra negative charges arising from the tensile stress at the interface, and therefore higher voltage than that of the new process would be required for turning on the P-TFT. In order to screen the effect of the dopant (boron in this case) on MILC, MILC was conducted before IMD on the source and drain, and the gate was also formed before

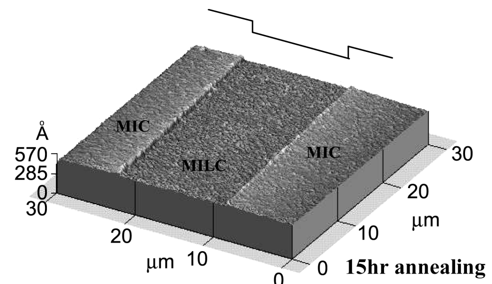

Fig. 6. AFM image of MILC area showing volume shrinkage after the crystallization.

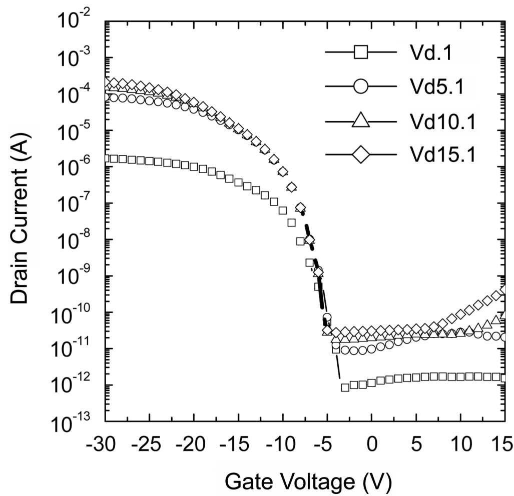

Fig. 5. I-V curves of P-TFT with a fabrication sequence of gatation + IMD + MILC.

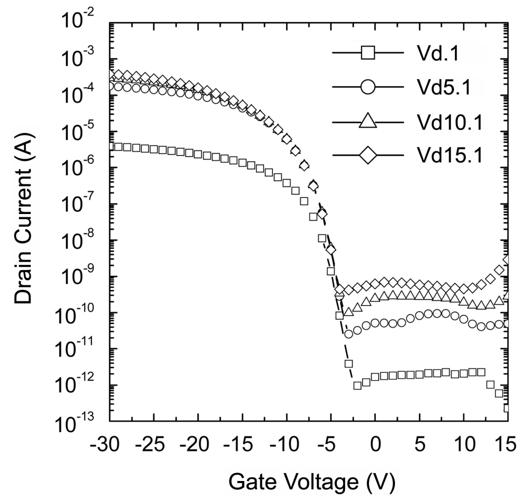

Fig. 7. I-V curves of P-TFT fabricated with the process sequence of gatation+MILC+IMD.

Table 2. Electrical parameters of Fig. 5.

	Vth	Swing	Mobility	On Current	Off Current	On/Off
10b×10	-9.5	0.48	21.65	$9.21*10^{-5}$	$2.75*10^{-10}$	334909

Table 3. Electrical parameters of P-TFTs, gate first, MLC later, and finally doping

	Vth	Swing	Mobility	On Current	Off Current	On/Off
10×10	-8	0.76	55.67	$2.99*10^{-4}$	$2.71*10^{-10}$	$3.03*10^{6}$

MILC. Thus, while the stress still exists in this case the channel crystallization was conducted without any dopant on the source and drain. The I-V curve of the thus fabricated P-TFT is shown in Fig. 7 and the electrical parameters are summarized in table 3. It should be noticed that the stress is responsible for the high threshold voltage and leakage current but has no relation with the electron moblility.

4. CONCLUSIONS

The processes proposed in this work were employed for fabrication of MILC TFTs, which show an electron mobility of 54 cm^2/V Sec, leakage current of $3.64*10^{-11}$, 30~40 pA and an on-current of $3.19*10^{-4}$. These values are typical in P-TFTs thus fabricated and are quite acceptable for most AMLCD and AMOLED applications. The main concepts of the new fabrication processes are as follows: 1) completion of crystallization prior to formation of the gate in order to eliminate the volume stress induced by volume change during metal induced lateral crystallization; and 2) formation of the source and drain after crystallization by ion mass doping followed by electrical activation at a temperature of 550 ^oC for 1 hour in a hydrogen ambient.

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