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Trap States of a-ZnO Thin Film Transistors

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We have investigated the stability of ZnO thin film transistors after application of positive gate bias stress and light illumination. We have observed a positive shift of the transfer curve after positive gate bias stress and a negative shift after light illumination. The recovery characteristics were observed by isochronal annealing after stress. After isochronal annealing, we could categorize the recovery into two types; recovery below 100°C, and that at around 125°C. The low temperature recovery was attributed to the trap charges and is consistent with the absence of variation of the sub-threshold slope with annealing temperature. The high temperature recovery at around 125°C was attributed to the presence of trap states mediated by hydrogen diffusion and is consistent with the observation of a sub-threshold slope increase with increasing annealing temperature. We conducted isochronal annealing analysis on oxide TFTs for the first time, and identified two kinds of stabilities: one is charge trapping and the other is trap states creation which are annealed out at around 125°C.

Keywords: oxide TFT, stability, ZnO, isochronal annealing

1. INTRODUCTION

Silicon based amorphous TFTs (thin film transistors) are widely used in information displays. With increasing pixel numbers and display size, oxide based TFTs are receiving much interest as they entail simpler processing steps and offer higher mobility than amorphous silicon TFTs. However, the application of a prolonged gate bias or light illumination results in a threshold voltage shift in oxide TFTs. ZnO TFTs also have been studied and their stability under gate bias stress and light illumination was reported. The good stability of TFTs is of great importance for their application to electronic devices including AMOLEDs (active matrix organic light emitting displays). Although oxide based TFTs have been extensively studied by a number of groups, there have been few reports on experimental investigation of the stability of oxide based TFTs.

It was reported that the application of positive and negative stress to ZnO TFTs resulted in positive and negative shifts of the transfer characteristics with sub-threshold slope degradation, respectively, and the characteristics recovered to near-original values at room temperature, which were attributed to charge trapping into the defect states within the band gap and band tails.[1] A bias stress experiment with IGZO (InGaZnO) TFTs showed that a positive gate bias resulted in a positive shift in the threshold voltage while the shift was small for a negative gate bias, and the time evolution of threshold voltage was described by a stretched exponential equation.[2] A report on the gate bias stability of a ZnO TFT under visible light illumination showed that light illumination accelerates the bias instability for negative gate bias stress, and this was attributed to charge trapping of photo-generated holes.[3] Since the thin film is sensitive to the surface states, adsorption and desorption have been studied in connection with the stability of the oxide TFTs.[4,5]

It was found that hydrogenation of ZnO at elevated temperatures gives rise to n-type conductivity.[6,7] and it was subsequently revealed by first-principles calculations that isolated hydrogen in ZnO acts as a shallow donor.[8] The experiments showed that bond-centered hydrogen (H_{BC}), primarily bound to the O atom with the O-H bond aligned parallel to the c axis, is a shallow donor and unstable against thermal treatment at 190°C.[9] Recently, it was reported that H_{BC} migrates through the ZnO and forms electrically inactive H_2. That is, the hidden hydrogen in ZnO occurs in the form of interstitial H_2.[10]

Although there have been reported on the structural, electrical, and optical properties of oxide transistors and materials,[11,12] there have been only a few reports on the stability of oxide TFTs and on recovery characteristics after degradation of oxide TFTs, respectively. In this work, we investigated recovery characteristics of ZnO TFTs by isochronal annealing after application of gate bias stress and light illumination and thereupon identified two types of instability.

2. EXPERIMENTS

Top gate ZnO TFTs were prepared on ITO coated glass.

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First, source and drain electrodes were defined by a photolithographic process. The thickness of the ITO was 130 nm. Following this, a 20 nm ZnO layer and a first gate insulator were deposited sequentially by ALD (atomic layer deposition). After formation of the active region by etching of the first gate insulator and ZnO, a second gate insulator was deposited to a thickness of 160 nm. Aluminum oxide was used for both the first and second gate insulator layers. For the top gate electrode, ITO was deposited by sputtering. The width and length of the fabricated TFT were both 10 μm. The cross-sectional structure of the TFT is shown in Fig. 1.

For measurement of the effects of bias stress and light illumination, the TFT was placed in a built-in heating element inside a vacuum chamber. We measured transfer characteristics after applying gate bias stress or light illumination. During gate bias stress or light illumination the drain and source electrodes were grounded. The effects of both the positive gate bias and light illumination on the transfer characteristics were investigated. We used a tungsten halogen lamp for the white light illumination.

After the transfer characteristics were shifted by the gate bias stress or light illumination, they recovered to the original state under various annealing temperatures. For investigation of the recovery characteristics after bias stress or light illumination, isochronal annealing has been used in previous studies.[13-16] In the present work, after bias stress or light illumination at 60°C, the transfer characteristics were measured at the same temperature of 60°C. We compared the results with the transfer characteristics after annealing for 1 hr at various annealing temperatures in a range from 60°C to 200°C. After annealing at each temperature, the temperature was decreased to 60°C and the transfer characteristics were measured for comparison: this is known as the isochronal annealing method. The above procedure was repeated for various gate bias voltages such as, 4 V, 8 V, and 12 V and under light illumination.

3. RESULTS AND DISCUSSIONS

Figure 2 shows the transfer characteristics for various stress times during application of positive gate bias stress. The gate bias stress was 4 V and the drain and source were grounded during the gate bias stress. Transfer characteristics were measured at a drain voltage of 0.5 V. With positive gate bias stress, the transfer curve moved to the right, which is consistent with the results of other groups.[1,17] With increasing stress time, threshold voltage increases. We also measured the effect of the gate bias stress for various gate biases. The change of the threshold voltage was larger for higher gate voltages.

As shown in Fig. 2, the sub-threshold slope of the transfer curve becomes slightly gradual after prolonged gate bias stress. For comparison of the slope, we drew two parallel guided straight lines at the sub-threshold regions. Since the sub-threshold slope is related to the trap states and becomes gradual with an increase of trap sites, we can conclude that the trap states as well as trap charges increase during positive gate bias stress.

Figure 3 shows the effect of annealing on the transfer characteristics. Transfer characteristics were measured at 60°C after annealing at each temperature up to 200°C. Annealing time at each temperature was 1 h. With increasing annealing temperature, the transfer characteristics recovered to the initial state. The recovery of the ZnO TFT after gate bias stress was reported by R. B. M. Cross et al. They observed that transfer characteristics degraded under positive gate bias stress recovered to near-original characteristics upon a short period of relaxation.[1] They suggested that the ZnO channel layer and/or the interface between the ZnO and the gate insulator layers are susceptible to charge trapping/defect formation instabilities due to lattice mismatch. However, the trend for sub-threshold slope degradation by gate bias stress is still not clear.

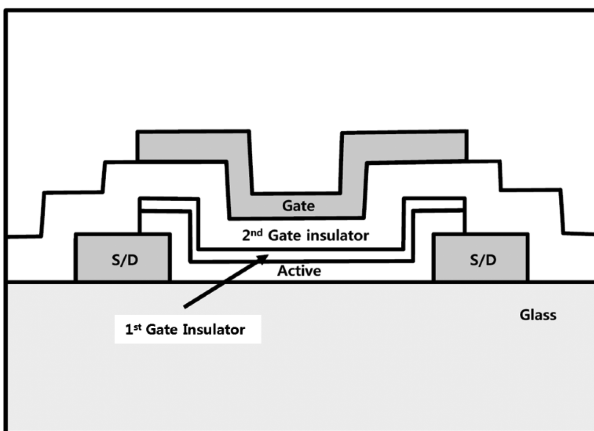

Fig. 1. The cross-sectional structure of the fabricated top gate ZnO TFT.

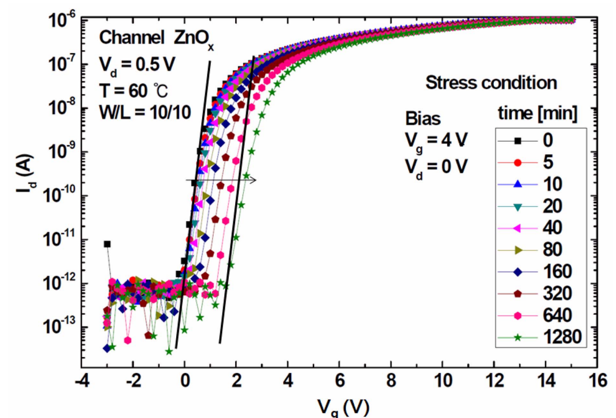

Fig. 2. Transfer characteristics of the fabricated ZnO TFT were measured during positive gate bias stress at 60°C. Two guided straight lines at sub-threshold region are parallel each other.

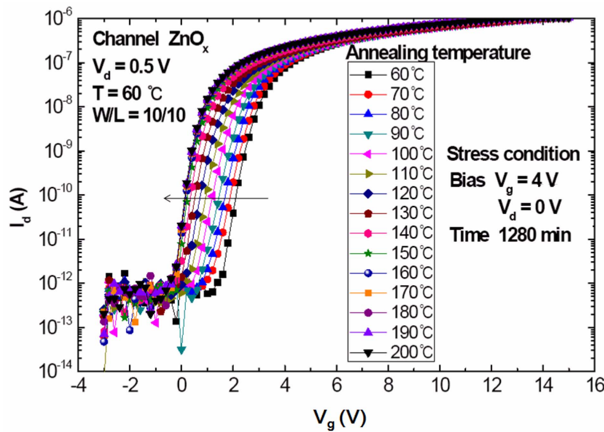

Fig. 3. Recovery of the transfer characteristics as increasing the annealing temperatures.

In the case of an a-Si:H TFT, it is known that charge trapping and the creation of dangling bonds increase the threshold voltage, which is recovered by annealing at a temperature of around 160°C. Isochronal annealing study of *a*-Si:H TFTs showed that threshold voltage recovery at low temperatures below 90°C occurs by charge de-trapping, whereas the recovery around 160°C is associated with annealing of the bulk dangling bonds and that at around 110°C was attributed to annealing of the interface defects.[13-16] In an *a*-Si:H TFT, the increased defect states by gate bias stress are dangling bonds, which are created by hydrogen assisted bond breaking after electron or hole trapping into the weak Si-Si bond. However, the behavior and the origin of the defect states are not clear in oxide TFTs.

In Fig. 3, we can observe the recovery of the sub-threshold slope as well as the threshold voltage. Isochronal annealing after bias stress was repeated for gate bias stresses of 4 V, 8 V and 12 V. In these isochronal experiments, we obtained similar recovery rate behaviors, as shown in Fig. 4. The graph shows the recovery rate of the threshold voltage according to the annealing temperature. With increasing annealing temperature, the threshold voltages decrease to the original values. The recovery rate is given by the threshold voltage difference ($V_{th(n)} - V_{th(n-1)}$) divided by the temperature difference ΔT. An uneven recovery rate of the threshold voltage was observed as also found in the case of isochronal annealing of a-Si:H TFTs after gate bias stress or light illumination.[13-16] As shown in Fig. 4, the mechanism of the recovery rate can be divided into two groups, recovery below 100°C and recovery at around 125°C. The recovery below 100°C can be attributed to de-trapping of the trap charge. However, the recovery at around 125°C is rather high and is not due to the charge de-trapping.

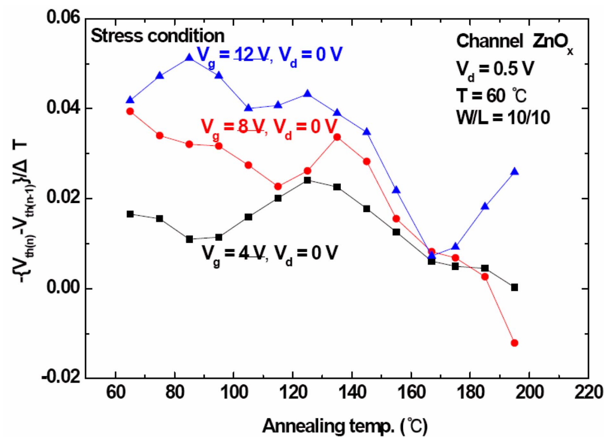

Fig. 4. Recovery rate of the threshold voltages as a function of annealing temperatures.

Figure 5 shows the transfer characteristics after white light illumination. The effect of light is very large. The high sensitivity and large threshold voltage shift by light illumination observed here were also previously reported for oxide materials and TFTs.[3,18-20] Fast negative shift of the threshold voltage by light illumination is a common characteristic of oxide TFTs. Previous studies have attributed light induced instability to photo-generated holes or oxygen adsorbed at the surface.[3,4]

Isochronal annealing temperature dependence of the recovery after light illumination is shown in Fig. 6. At low temperatures, the recovery is fast and the sub-threshold slope does not change. For comparison of the slopes we drew parallel straight lines at the sub-threshold region. However, at higher temperatures, the sub-threshold slope changes with increasing annealing temperature. The sub-threshold slope is associated with trap states between the Fermi level and conduction band edge. The increased number of trap states results in gradual slope of the sub-threshold region. Therefore, the recovery at higher temperatures over 100°C can be attributed to a decrease of trap states. This is clearer at the recovery rate shown in Fig. 7.

Recovery rates are grouped into two groups, recovery below 100°C and recovery at around 125°C. Annealing at

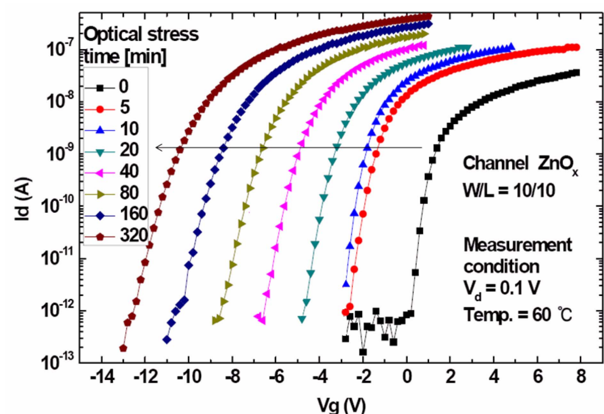

Fig. 5. The effect of white light illumination.

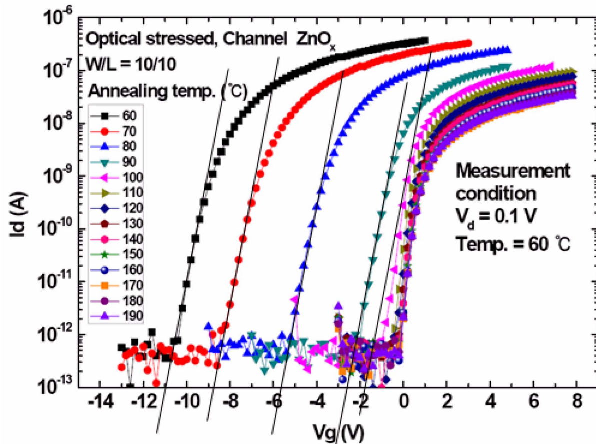

Fig. 6. The recovery characteristics by isochronal annealing after light illumination. Straight lines at sub-threshold region are all parallel.

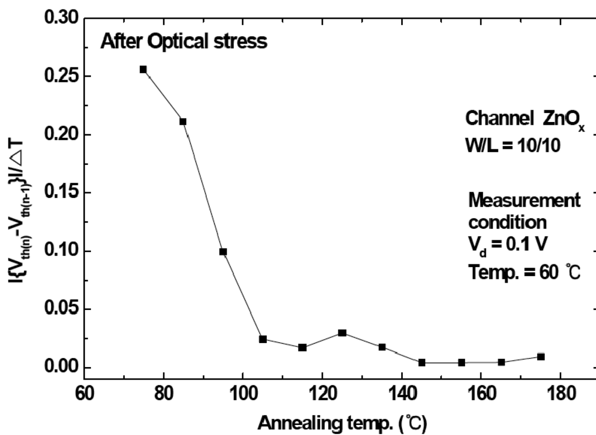

Fig. 7. Recovery rate during isochronal annealing after light illumination.

roughly 125°C neither causes charge de-trapping nor a decrease of trap states, which is associated with the sub-threshold slope change, as shown in Fig. 6. The temperature dependence of the recovery rate is consistent with the change of the sub-threshold slope, which decreases at temperatures over 100°C, as shown in Fig. 6. In Fig.4, the change of the trap states during recovery after gate bias stress can be observed. The recovery rate peak at around 125°C after light illumination is consistent with the recovery rate peak after positive gate bias stress, as shown in Fig. 4, and the values of the recovery rate for the positive bias and light illumination are similar.

Light illumination generates electrons and holes while positive gate bias leads only to the accumulation of electrons. Therefore, the drastic negative shift of transfer characteristics can be attributed to holes or the combined effect of holes and electrons. Most of the change at low temperatures below 100°C can be attributed to charge trapping, as indicated by the low recovery temperatures and the parallel shift of the sub-threshold region. The charge trapping in light illumination can be understood by the similar valence band energy position of ZnO to the gate insulator due to the deep valence level of ZnO from the vacuum level. A small hole barrier facilitates hole trapping at the gate insulator. Moreover, if an internal field is formed at the gate insulator due to the non-zero flat band voltage, large hole concentration by light illumination could promote rapid hole trapping to the gate insulator. The trapped charge can be de-trapped easily, resulting in a parallel shift of the sub-threshold region, as shown in Figs. 6 and 7.

The annealing peak at approximately 125°C after light illumination is associated with trap centers, which correspond to the trap centers after positive gate bias stress. During isochronal annealing after positive gate bias stress, trap charges and trap centers decrease and they can be differentiated by annealing temperature, as shown in Fig. 4. Charge de-trapping occurs relatively low temperatures below 100°C. Therefore, we can conclude that electrons at the ZnO layer by positive gate bias create trap states between the Fermi level and the conduction band edge as well as trapped charges. Light illumination creates electrons as well as holes, and therefore, we can draw the same conclusion regarding the creation of trap states between the Fermi level and conduction band edge during light illumination. However, it is not clear whether holes create trap states in this experiment.

In the case of a-Si:H TFT, the creation and annealing of defect states are associated with hydrogen, and the diffusion rate of hydrogen plays an important role in defect creation and annealing. In ZnO, it is known that hydrogen acts as a donor. Furthermore, the diffusion of hydrogen in crystalline ZnO was recently analyzed by isochronal annealing, and it was revealed that the interstitial hydrogen anneals out via diffusion of hydrogen. The highest annealing rate was observed at around 135°C.[9] This diffusion temperature is similar to the recovery peak after positive bias or light illumination in ZnO TFTs considering crystalline ZnO in the hydrogen diffusion experiment.

There are several defects that are suspected as donor states, such as Zn interstitials, oxygen vacancies and hydrogen. Since hydrogen diffusion is more easy compared to Zn and oxygen and the diffusion temperature of hydrogen is similar to the annealing peak of the recovery in ZnO TFT, based on the findings of isochronal annealing experiments, we suggest that hydrogen mediated trap states can be created by gate bias stress and light illumination. In addition, we can classify the origin of the stability of ZnO TFTs into two types, charge trapping presented with low temperature annealing below 100°C and trap states between the Fermi level and tail states, presented with annealing temperature around 125°C.

4. SUMMARY

We conducted experiments of gate bias stress and light illumination on ZnO TFTs. After degradation of the characteristics by positive gate bias stress or light illumination we made recovery experiments by isochronal annealing. We observed positive shift of transfer characteristics after positive gate bias stress and negative shift after light illumination.

After isochronal annealing, we could categorize the recovery into two types, recovery below 100°C, and the recovery at around 125°C. The low temperature recovery was attributed to charge trapping, and the high temperature recovery around 125°C was attributed to the creation of trap states mediated by hydrogen diffusion. However, further experiments are necessary to clarify the origin of trap states of ZnO TFTs and more elaborate isochronal experiments should be conducted to reveal the origin of the stability of the oxide TFTs.

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