Electronic Materials Letters, Vol. 2, No. 3 (2006), pp. 183-194

Review of Electrically Conductive Adhesive Technologies for Electronic Packaging

Myung Jin Yim[1,*] and Kyung Wook Paik[2]

[1]School of Materials Science and Engineering, Georgia Institute of Technology 771 Ferst Drive, Atlanta GA 30345, U.S.A.
[2]Deptartment of Materials Science and Engineering, KAIST 373-1, Kusong-dong, Yusong-gu, Daejeon 305-701, Korea

Conductive adhesives (ICAs; Isotropic Conductive Adhesive, ACAs; An-isotropic Conductive Adhesive & NCAs; Non-conductive Adhesive) offers promising Pb-free process and material solutions for electronic packaging technology to be fine pitch interconnects, low cost and low temperature process and environmentally clean approaches. ICA has been developed and used widely for traditionally solder replacement, especially in surface mount devices and flip chip application. It also need to be lower cost and higher electrical/mechanical and reliability performances. ACAs have been widely used in flat panel display modules to be high resolution, light weight, thin profile and low power consumption in the film forms (Anisotropic Conductive Films; ACFs) for last decades. Multi-layered ACF structures such as double and triple-layered ACFs were developed to meet fine pitch interconnection, low temperature curing and strong adhesion requirements. High mechanical reliability, good electrical performance at high frequency level and effective thermal conductivity for high current density are some of required properties for ACF materials to be pursued for wide usage in flip chip technology. Recently, NCAs are becoming promising for ultra-fine pitch interconnection and low cost joining materials in electronic packaging applications. In this paper, an overview on the recent development and applications of conductive adhesives for electronic packaging with focus on fine pitch capability, electrical/ mechanical/thermal performance and wafer level package application are described.

Keywords: conductive adhesives, electronic package, fine-pitch joint, flat panel display, flip chip, reliability, wafer-level package

1. INTRODUCTION

Today, resin based interconnection materials for electronic packaging and interconnection technologies are widely used in manufacturing of electronic devices such as flat panel displays and semiconductor/system package modules[1]. They are attractive as traditional solder alternatives due to advantages of low temperature and low cost process, finer pitch capability and environmentally clean solutions. Conductive adhesives are generally composite materials composed of insulating adhesive binder resin and conductive filler. Depending on the conductive filler loading level, they are divided into ICA and ACA or NCA. For ICA, the electrical conductivity in all x-, y- and z-directions is provided due to high filler content exceeding the percolation threshold. For ACA or NCA, the electrical conductivity is provided only in z-direction between the electrodes of the assembly. Figure 1 shows the typical structures of ICA, ACA and NCA flip chip joints illustrating the bonding mechanism for all three adhesives. Especially, ICA materials, typically silver-filled conductive adhesives have been recommended as solder replacement materials in SMT, flip chip, chip scale package (CSP) and ball grid array (BGA) applications. There are still challenging technical issues for full commercialization of ICAs such as lower conductivity and reliability, high material cost, and poor impact strength, etc. and extensive research works are being performed to enhance the electrical performance and reliability of adhesive joints[2-6].

Interconnection technologies using ACFs are major packaging methods for flat panel display modules to be high resolution, light weight, thin profile and low consumption power[7], and already successfully implemented in the forms of Out Lead Bonding (OLB), flex to PCB bonding (PCB), reliable direct chip attach such as Chip-On-Glass (COG), Chip-On-Film (COF) for flat panel display modules[8-11], including LCD, Plasma display panel (PDP) and organic light emitting diode display (OLED). As for the small and fine pitched bump of driver ICs to be packaged, fine pitch

*Corresponding author: myim3@mail.gatech.edu

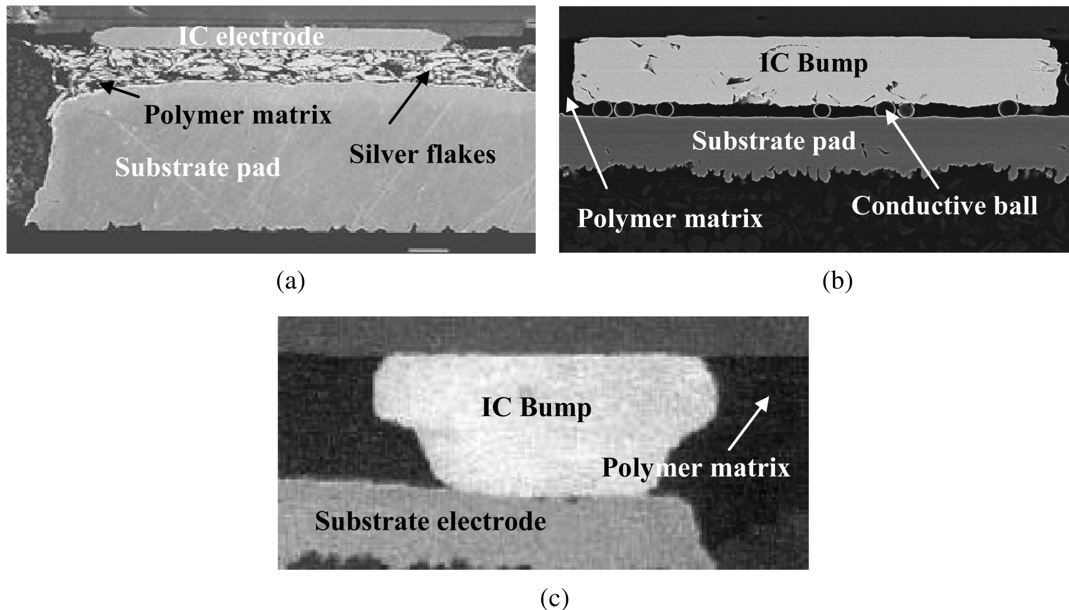


Fig. 1. Cross sectional views of (a) ICA, (b) ACA and (c) NCA flip chip bonding.

capability of ACF interconnection is much more desired for COG, COF and even OLB assemblies. There have been advances in development works for improved material system and design rule for ACF materials to meet fine pitch capability and better adhesion characteristics of ACF interconnection for flat panel displays. Alternative resin based interconnection materials such as anisotropic conductive pastes (ACPs) and non-conductive films/pastes (NCFs/Ps) have been developed and introduced due to their advantages in terms of process, cost and ultra-fine pitch capability where conventional ACF has limitation.

It is obvious that conductive adhesive materials are being more required for advanced packaging materials, but formulation, material design and process should be optimized and developed for high electrical, mechanical and thermal performance as well as enhanced reliability performance.

In this paper, an overview on recent issues, development and applications of conductive adhesives for electronic packaging applications with fine pitch capability, high electrical, mechanical, and reliability performance, and wafer level flip chip package applications is described.

2. ISOTROPIC CONDUCTIVE ADHESIVES (ICAS) FOR ELECTRONIC PACKAGING

ICAs are being used to replace the traditional eutectic SnPb solder alloys in electronic packaging and interconnects. They are composites of polymer resin and conductive fillers. The polymer resins, thermoplastic or thermosetting resins, are generally cured at high temperature and provides the shrinkages force, adhesion strength, good chemical and corrosion strength. Epoxy, cyanate ester, silicone, polyurethane are thermosetting resins, and phenolic epoxy, polyimide are common thermoplastics for ICA matrix resin. Conductive fillers include silver (Ag), gold (Au), nickel (Ni), copper (Cu) and Sn, SnBi or SnIn coated Cu in various sizes and shapes. Ag is the most common conductive fillers for ICA due to high conductivity and easy process, but its high cost is one of drawbacks for wide use of Ag-filled ICAs. ICAs have been used for die attach adhesives[12-13], adhesives for SMT[14-15], and flip chip[16] and other applications. Figure 1 shows the schematics of SMT components and flip chip devices interconnected by ICAs instead of solder alloy.

However, current ICAs still have some limitations on the electrical, thermal, and reliability properties compared with SnPb solders for full replacement for solder. Table 1 shows a general comparison in various properties between SnPb solders and conventional ICAs[17].

Therefore, many research efforts have been focused on the improvement of electrical conductivity of ICAs and reliability enhancement of ICA joints, electrically and mechanically. Also the replacement of expensive Ag flakes into new metal flakes is required for wide use of ICAs instead of solder materials. Copper can be conductive filler metal due to its low resistivity, low cost and improved electromigration performance, but oxidation causes this metal to lose its conductivity[18].

2.1. Electrical conductivity improvement of ICAs

To enhance the electrical conductivity of metal-filled ICAs, polymer-metal composite properties are controlled and maximized. Typically, increasing cure shrinkage of

Table 1. Comparison between Conducvtive Adhesive and Eutectic Solders

Characteristics	SnPb solder	ICA
Volume resistivity (Ωcm)	0.000015	0.00035
Typical junction R (mΩ)	10-15	<25
Thermal conductivity (W/mK)	30	3.5
Shear strength (psi)	2200	2000
Min. processing temperature (^{o}C)	215	150~170
Environmental impact	Negative	Very minor

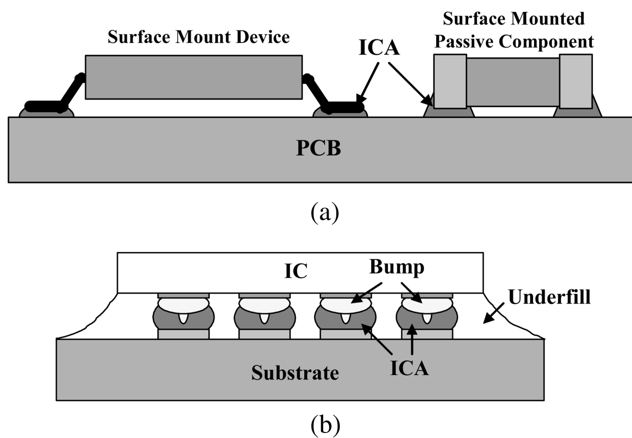


Fig. 2. Schematic structures of (a) surface mount interconnection using ICA, and (b) flip chip interconnection using ICA.

matrix polymer binder[19], the intimate metallic contacts by removal of lubricant layer on Ag flakes[20], and oxidative layer removal[21], metallurgical bonding between the conductive particles by low melting point alloy coating on Cu powder[22-23] are representative methods for improvement of ICA conductivity. Recently, nano-sized Ag particles are added as conductive fillers instead of highly loaded micron-sized Ag flakes and sintering of nano-sized Ag fillers enhances the electrical conductivity[24].

2.2. Reliability Enhancement of ICA Interconnects

Critical reliability concerns of ICA joints in electronic packaging applications are mainly due to unstable contact resistance between ICA and metal finished components under environmental attacks, such as humidity and temperature cycling/aging. For high temperature and humidity aging environment, the galvanic corrosion rather than simple thermal oxidation at the interface between metallic fillers in ICA and non-noble metal finish is known as the mostly detrimental underlying mechanism for unstable contact resistance[25]. Therefore, most research works for improving the stability of electrical conductivity of ICA joints are related to the methods of avoiding or minimizing the unstable contact resistance mechanism of ICA joints. Several methods are development of polymer matrix resin with low moisture absorption[26], uses of oxygen scavenger[25] and corrosion inhibitors[26] in the ICA formulation, the corrosion control by adding of low corrosion potential individual metals, sacrificial anode[27], and oxide-penetrating particles in the ICA formulation[28]. Also, for the reliability improvement of Ag-based ICA joints, Ag migration is most serious concern. Several methods are proposed to reduce Ag migration and improve the reliability of ICA joints such as Ag alloying with an anodically stable metal[29], hydrophobic polymer coating over the PWB[30], surface coating of tin, nickel, gold or organic compounds on silver particles.

Under thermal cycling (TC) environment, the failure mechanisms of unstable ICA performances are generally the thermal stress in the ICA joints and the interfacial delamination due to the adhesion degradation. The TC performance of ICA joints can be improved by reducing the thermal stress with flexible molecule in the epoxy resin[31], and by low CTE adhesive layer for reduced thermally induced shear strain[32].

3. ACAs FOR FLAT PANEL DISPLAYS

ACF materials are mostly wide used in connecting the tape-carrier packages (TCPs) with driver IC to the LCD glass panel and PCB boards, and other interconnection areas for flat panel displays manufacturing. Figure 3 shows various packaging technologies using ACF for LCD modules; TCP, COG and COF bonding. Since connection pitch of driver IC electrode has been decreased and the number of output electrodes per IC increased for the progress of high resolution LCD modules, ACF materials and packaging technologies have also been developed to meet high density interconnection capability.

ACF bonding process is thermo-compression bonding as shown in Fig. 4. In case of TCP bonding, ACF material is attached on glass substrate after release film removal and TCP with driver IC is pre-attached. Then final bonding is established by thermal cure of ACF resin, typically at 180 ^{o}C, 20 seconds and 30 kg_f/cm^2 and conductive particle deformation between the electrodes of TCP and glass substrate by applied bonding pressure.

The kind, size, density of conductive filler, and adhesive

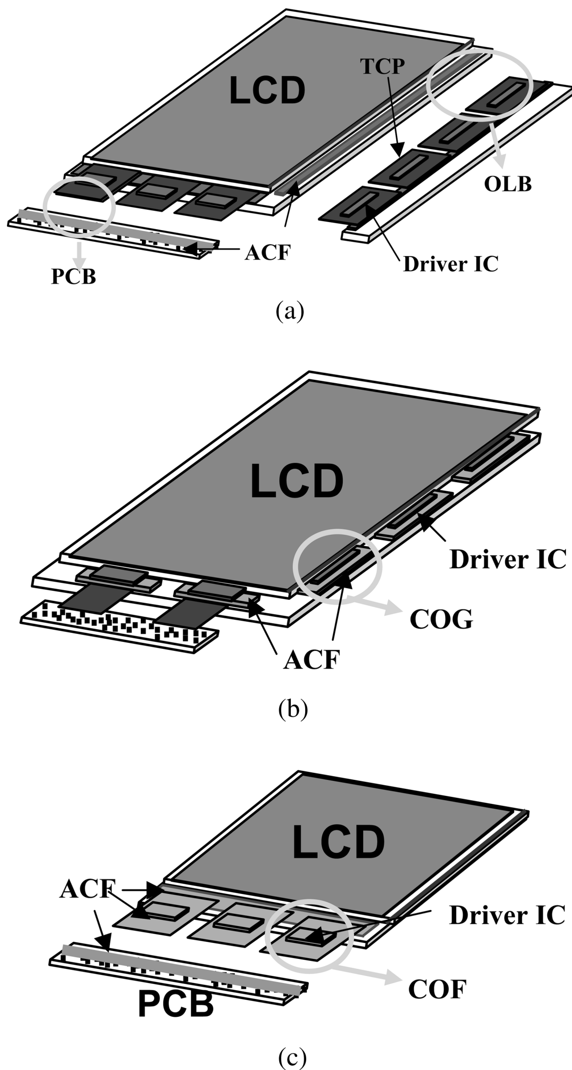


Fig. 3. Various packaing technologies using ACF in LCD modules (a) TCP; Outer Lead Bonding (OLB) and PCB bonding, (b) COG bonding and (c) COF bonding.

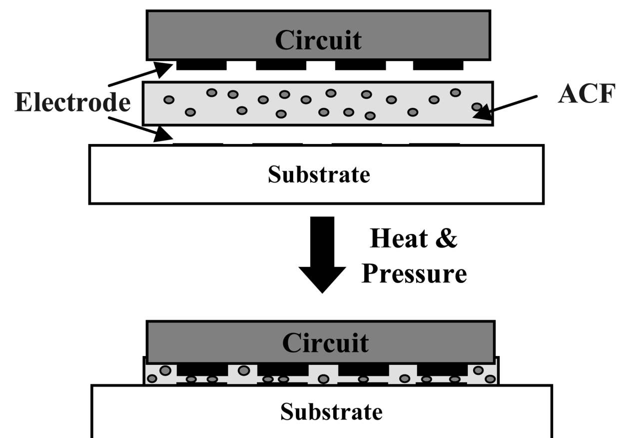


Fig. 4. Thermo-compression bonding using ACF.

resin system are different according to packaging technologies for LCD module. When TCP is mounted using ACF on LCD glass substrate, the CTE mismatch between TCP and the panel should be considered for thermal bonding, and this is more serious for finer pitch TCP bonding below 50 μm. For flex to glass bonding below 50 μm pitch, COF using ACF become more popular due to several advantages like fine pitch capability, design flexibility and low CTE base material. ACF are also used in attaching fine-pitched driver IC on COF substrates. The geometry of COF is very similar to that of TCP. However the substrate is different, that is two-layer structure, normally Cu and polyimide (PI) which is thinner, higher density, better flexible and more durable in high temperature than TCP with three-layer structure (Cu, adhesive and PI). COF's two-layer structure without adhesive layer is normally weak adhesion property with ACF materials. Therefore, there has been development in ACF adhesion improvement to two-layer COF substrate.

In COG technology, the bare driver ICs are flip chip bonded on glass substrate using ACF, and it is most advantageous technology for low cost and compact size LCD module production[33]. The CTE difference between driver IC and glass substrate is relatively small compared with that in TCP applications and it provides more reliable COG connections.

4. ACFs FOR FINE PITCH INTERCONNECTION

As the function of driver IC for high-resolution LCD module increases, the bump density on IC also becomes increased and this mean bump size and pitch are reduced. For fine pitch COG connection using ACF, the number of conductive particles trapped between the bump and substrate pad should be enough. Therefore, conductive particle density of ACF for COG is much higher than that of ACF for TCP OLB. But due to high density of conductive particles, there is high possibility of electrical short between adjacent bumps, mainly due to conductive particle accumulation by being flowed into the bump gap during COG bonding process. Therefore double-layer ACF, which composed of ACF layer and NCF layer without conductive filler, was developed to have high electrical conductivity between bump and ITO electrode and electrical insulation between adjacent bumps[34]. As bump size and pitch of driver IC is more and more decreasing, insulating layer coated conductive particle was introduced instead of conventional conductive particles in ACF layer, and non-conductive fillers were incorporated together with conductive particles to ensure electrical insulation[35].

Figure 5 shows the relationship between the short circuit rate and the type of conductive particle. The double-layer

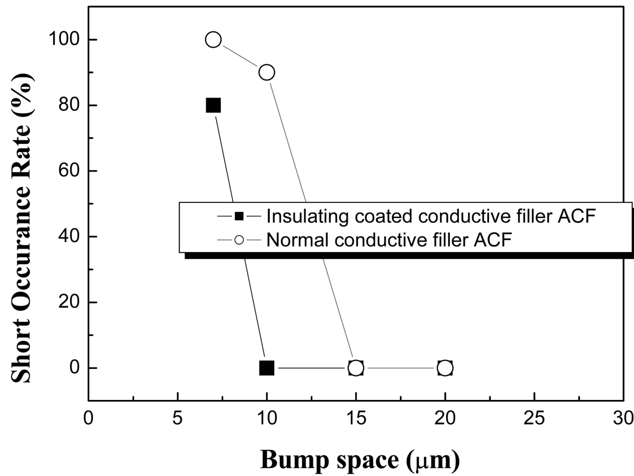
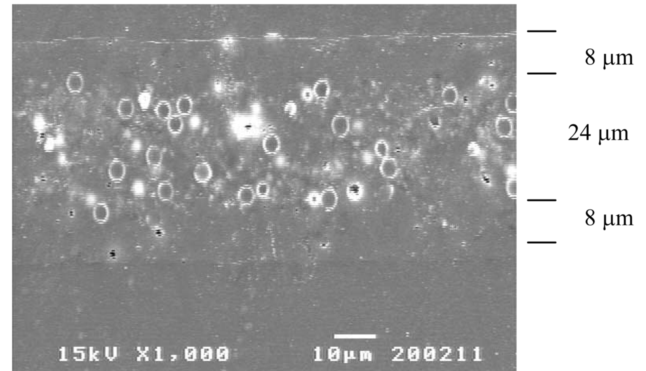


Fig. 5. The relationship between the short circuit rate and the type of conductive particle.

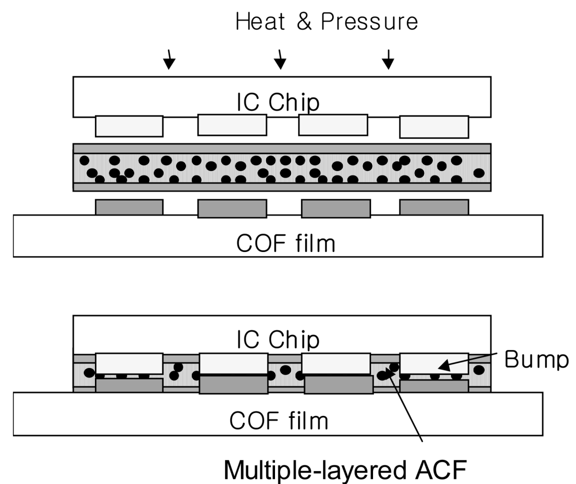
ACF with conventional conductive particle and insulating layer coated conductive particle, both in in 4 μm diameter size and 35,000/mm^2 density. Insulating coated conductive filler ACF is more advantageous than normal conductive particle ACF by reducing electrical short more effectively, and it achieved insulation capability at 10 μm gap level. In double-layer ACF structure, ACF and NCF layer thickness are 7 μm and 18 μm, respectively. The viscosity, formulation, thickness of adhesive layers, conductive filler density, type and hardness should be optimized for high performance COG package.

COF, another fine pitch ACF bonding area, is relatively new technology compared with COG and COB in the production of flat panel module. LCD module production using COF technology is in up-growing stage due to its advantages of fine-pitch interconnection, low contact resistance and pre-test capability compared with COG in the high-density, multi-functional LCD module. In COF technologies, there are several alternatives for interconnect materials and processes, such as Au-Sn joining[36], stud bump bonding (SBB) joining[37], ACF joining[38], NCF and NCP joining[39]. Among them, ACF joining method has been applied as main bonding method similar to COG technology.

As aforementioned, COF's substrate is two-layer structure without adhesive layer, and therefore is normally weak adhesion property with ACF materials. It is necessary to improve the adhesion property between IC chip, ACF and two-layer flex substrate for ever-increasing reliability requirement of COF module. In addition, fine-pitch interconnection is the basic requirement in COF using ACF for driver IC packaging. Triple-layered ACF has been developed, which has functional layers on both side of conventional ACF layer to improve interface adhesion and control bonding property for fine pitch application during thermo-compression bonding



(a)



(b)

Fig. 6. (a) Cross-sectional view of triple-layered ACF by SEM and (b) COF bonding process using triple-layered ACFs.

as shown in Fig. 6, and the resulting reliability enhancement of COF module assembly[40].

5. ACAs FOR HIGHLY RELIABLE FLIP CHIP ASSEMBLIES

Flip chip assembly on organic board using anisotropic conductive adhesive (ACA) have received much attentions due to many advantages such as simple and lead-free processing, low cost, fine pitch interconnection and low temperature processing[41-43]. Especially highly improved electrical and thermal performance as well as high frequency characteristics are anticipated due to reduced interconnection distances.

Most of all, flip chip using anisotropic conductive adhesive should provide acceptable reliability level in harsh environment together with good processability. It requires the use of polymer materials that have close CTE value to the chip and the board, and strong adhesion for better reliability.

Table 2. Tg, CTE, and Modulus of ACA Composites

ACA composite	Tg^{TMA}(°C)	CTE (ppm/°C)		Modulus (GPa @25 °C)
		α1	α2	
ACA 1 with 10 wt% filler	87.62	87.9	3960	5.3
ACA 2 with 30 wt% filler	93.53	76.1	3630	3.2
ACA 3 with 50 wt% filler	98.77	60.7	3920	2.5

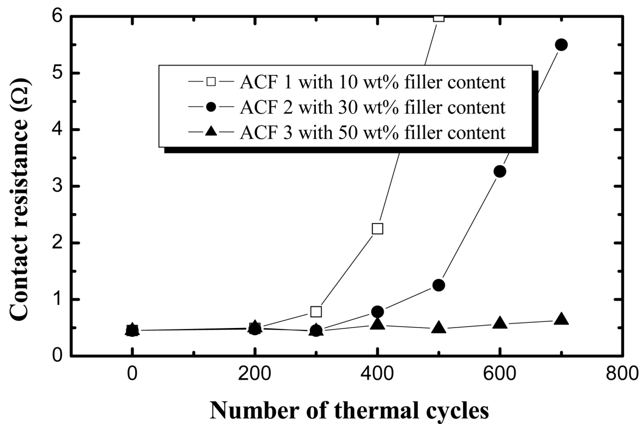


Fig. 7. Contact resistance of flip chip interconnects using ACA with different filler content during thermal cycling test from -60°C to 150°C for 700 cycles.

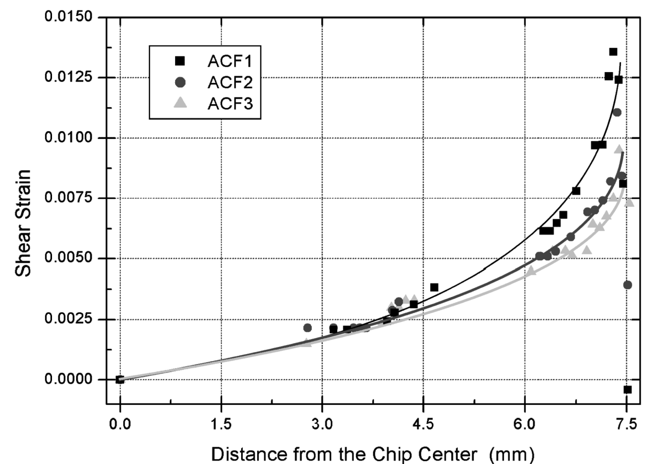


Fig. 8. Thermal shear strain of ACF layer between chip and FR-4 substrate of flip chip assembly.

For the better mechanical properties without degradation of strong adhesion, non-conductive fillers are incorporated and optimized. As the content of filler increased, CTE values were decreased and storage moduli were increased, but the DSC behaviors didn't change. Table 2 summarized the material properties of ACA composites with different filler content showing lower CTE and higher modulus as filler content increases.

For the test IC chip and substrate, the gold stud bumps were formed on each I/O pad of test chips and 1 mm-thick FR-4 substrates were prepared. Flip chip assembly was performed by bonding the chip on the substrate with an appropriate bonding pressure of 50 kg_f/cm^2 at 180 °C for 30 seconds. The chip was electrically connected to the substrate via the contacts between compressed gold stud bumps and conductive fillers in the ACA. Non-conductive fillers with smaller size than conductive fillers don't contribute the electrical contacts and instead affect other properties such as Young's modulus and CTE.

Reliability tests in terms of temperature cycling, high humidity and temperature, and high temperature and dry condition test were performed by measurement of contact resistance variation. Figure 7 showed that flip chip assembly using modified ACA composites with lower CTEs and higher modulus by loading non-conducting fillers exhibited better contact resistance behavior than conventional ACAs without non-conducting fillers. An ACF with a lower CTE and higher modulus can reduce the thermally induced shear strain in ACF layer measured by moiré interferometry during thermal cycling environment as shown in Fig. 8, and thus can increase the overall thermal cycling lifetime of ACF joints[44]. There are still more demanding issues for reliability enhancements such as low moisture absorption and interface stability of adhesive resin in ACA[45-46].

6. ACAs FOR HIGH FREQUENCY INTER CONNECTION

Recently, high frequency modeling and characterization for ACA flip chip interconnects have been performed to understand high frequency characteristic of flip chip interconnect using ACFs, and thereby design better ACF materials and bump system[51-53].

Effect of low dielectric filler addition on high frequency behavior of ACF was investigated. The extracted impedance model parameters of a 100 μm × 100 μm bonding pad were presented in Fig. 9 for conventional ACF with conductive ball only, and ACF with conductive ball and SiO_2 filler. In ACF flip chip interconnect at high frequency, interconnection capacitance formed between CPW of PCB and the test chip pad is relatively high due to the high dielectric constant of the ACF resin and the large area, small gap of the parallel metal plate structure, compared with the solder ball flip chip

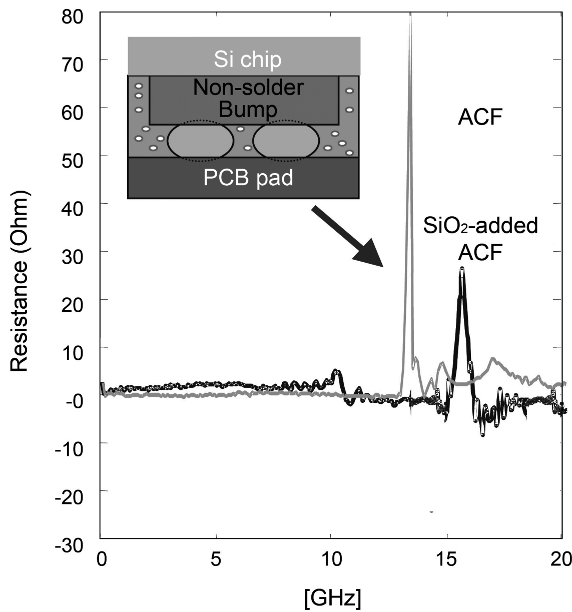


Fig. 9. Impedance parameters, resistance (R) of flip chip interconnect using electroless Ni/Au bumped chip and two different ACFs in high frequency range.

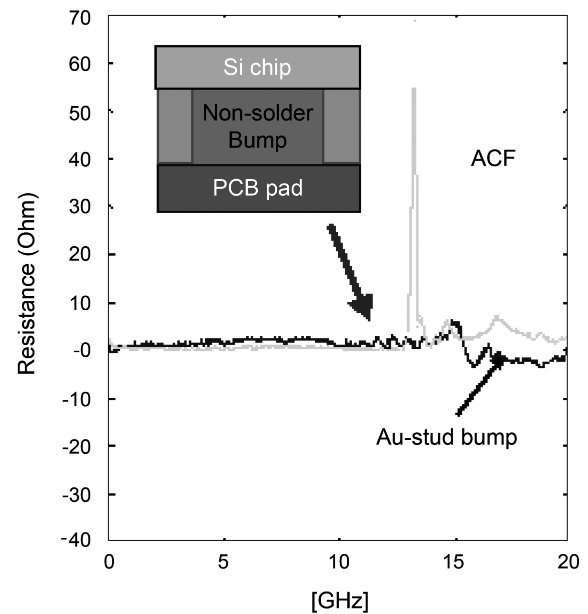


Fig. 10. Impedance parameters, resistance (R) of flip chip interconnect using ACF without silica and two different chips, electroless Ni/Au bumped and Au stud bumped chip in high frequency range.

structure. Therefore, the resonance frequency of the ACF flip chip interconnect is lower than that of the solder ball flip chip interconnect.

Both ACF have resonance frequencies, around 13 GHz for conventional ACF and 15 GHz for SiO_2 added ACF. This resonance phenomenon is dominantly affected by the inductance of conductive particle and capacitance of polymer matrix. In particular, capacitance of polymer matrix is induced by the proximity effect of chip and substrate. Interestingly, ACF with SiO_2 has resonance frequency slightly higher than conventional ACF. ACF including SiO_2 filler exhibited the resonance phenomena around 15 GHz. This difference is originated from dielectric constant change of polymer matrix. By adding SiO_2 filler into ACF formulation, dielectric constant of polymer matrix in ACF was lowered according to the result of ACF's dielectric property and resulted ACF resonance shifted to higher frequency.

Effect of bump metallurgy on high frequency behaviors of ACF interconnects was also investigated. Figure 10 shows the impedance parameters of Au stud bumped chip packaged by ACF method, and compared with Ni/Au bumped chip. As shown in Fig. 10, Au stud bumped chip did not exhibit resonant phenomena up to 20 GHz. This means that Au stud bumps maintain the constant impedance in high frequency range up to 20 GHz. Capacitive coupling of the Au-stud bump interconnect between chip and substrate is relatively low due to the large gap of epoxy resin and the small area in the parallel pad structure, compared to the ACF flip chip using Ni/Au bumped chip. Consequently, the resonance frequency of the Au stud bump interconnects using ACF is higher than that of ACF flip chip interconnect using electroless Ni/Au bump, and was not observed up to 20 GHz.

High frequency performances of several flip chip interconnects using ACFs at RF and high frequency range were demonstrated and ACF flip chip assembly was proved as a simple and cost effective method for high frequency devices [54].

7. ACAs FOR HIGH CURRENT DENSITY INTERCONNECTION

As the current density at the ACA flip chip assembly is increasing for high current and high power dissipation device applications, the current carrying capability of ACA is one of important properties and has been characterized [55]. ACA, normally thermally poor conductor, is required to be thermal transfer medium which allows the board to act as new heat sink for the flip chip package and improve the lifetime of ACA flip chip joint under high current density application. The effect of thermal conductivity of ACA on the current carrying capability of flip chip joints was investigated[56]. Figure 11 shows comparison result of I-V characteristics when ACA flip chip joints is bias-stressed at a pair of Au stud bumps/ACA joints between conventional ACA without any thermal filler and thermally conductive ACA with 100 phr SiC fillers. The conventional ACA flip chip joint shows the typical I-V curve with maximum allowable current level of 4.53 A. In contrast, flip chip joint using thermally conductive ACA shows almost linear increase of current as increase of voltage and maximum allowable current level is 6.71 A. Therefore the current carrying capability of

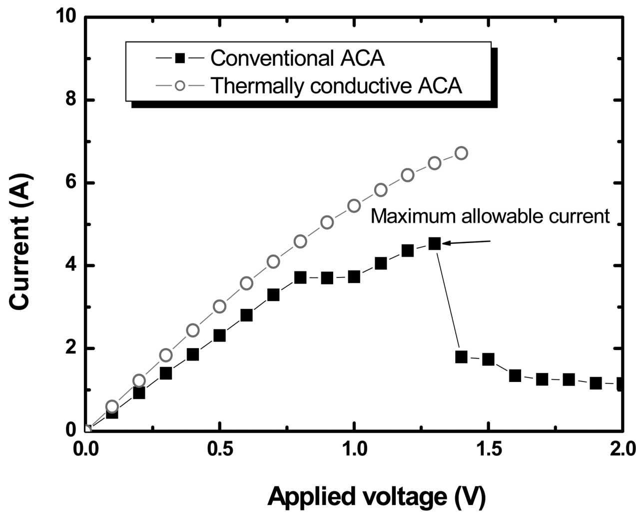


Fig. 11. I-V test (bias stressing) results at Au stud bumps/flip chip joints by conventional ACA and thermally conductive ACA.

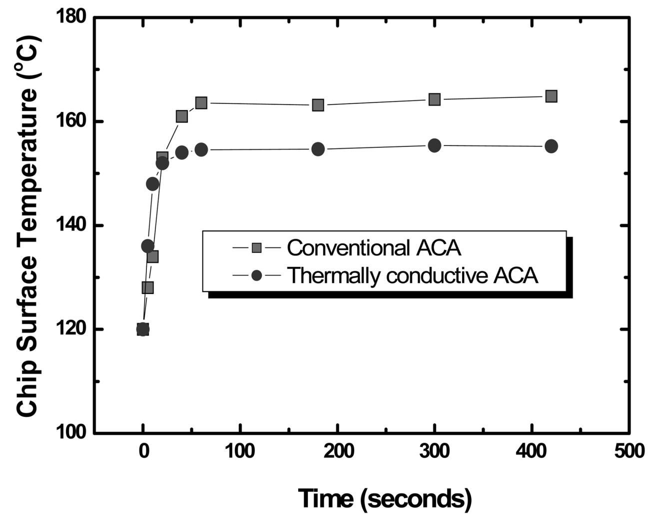


Fig. 13. Maximum chip surface temperature of flip chip assemblies using conventional and thermally conductive ACAs as a function of time under high current applying condition.

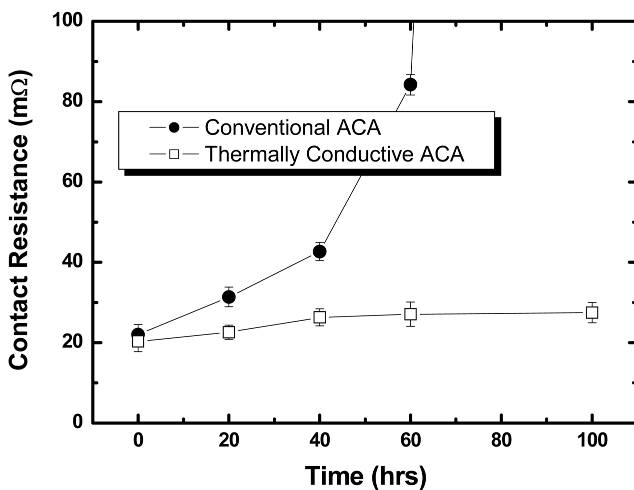


Fig. 12. Contact resistance changes of Au stud bump/flip chip joints using conventional ACA and thermally conductive ACA after 20, 40, 60, 100 hours under current stressing.

ACA flip chip joint was improved by the use of thermally conductive ACA material. Figure 12 shows the resistance changes of flip chip joints using conventional ACA and thermally conductive ACA as a function of time under constant current of 4.1 A. The contact resistances of conventional ACA flip chip joints increased abruptly as time passed 50 hrs and had open circuits before 100 hrs. But the thermally conductive ACA flip chip joints showed stable contact resistance behaviors without any open circuit. The failure or degradation mechanism of ACA flip chip joints under current biasing test are suggested as follows; (1) Au-Al IMCs formation, (2) Crack formation and propagation along the Au/IMC interface, and (3) Al or Au depletion due to electromigration[57]. All those causes of electrical degradation of ACA flip chip joints are caused by heat accumulation at the Au stud bumps/PCB pads and thermal degradation of adhesive due to joule heating under high current bias. Similar discussion on the heat induced failure mechanism of flip chip joint using isotropic conductive adhesive (ICA) under high current density was presented[58].

If the local temperature of flip chip joint by ACA/Au stud bump is relatively low due to effective heat dissipation throughout thermally conductive ACA, the thermally degradation process due to local joule heating and thermal degradation are slowed down, and electrical stability is obtained. This is verified by the behavior of junction temperature on the surface of flip chip IC assemblies under current stressing condition as a function of time in Fig. 13. The maximum chip surface temperature increases abruptly and become stable at around 50 seconds of high current applying time. The chip surface using thermally conductive ACA became hot faster than conventional ACA joint, which means thermally conductive adhesive dissipates the heat from the source more easily than conventional ACA does.

The maximum temperature of chip surface of flip chip joint using thermally conductive ACA is lower than that of conventional ACA under constant current stressing. Therefore, the electrical reliability of flip chip joint under high current bias condition can be improved by dissipating the heat from hot spot and keep the chip temperature as cool as possible.

8. ACAs FOR WAFER LEVEL PACKAGES

Flip chip technology is extending its applications to the fields of smart cards, displays, computers, mobile phones and communication systems, etc. However, the flip chip

technology has a drawback that the production efficiency is poor in terms of process complexity and product cost because it requires conventional solder-using complex connection processes, that is, solder flux coating, chip/board arranging, solder bump reflowing, flux removing, underfilling and cure process. In order to reduce these complex processes, particular attention has recently been paid to wafer-level packaging technology in which wafers are coated with polymeric materials having flux and underfill functions[59-60]. More recently, in developing new, improved flip chip connection technology, advantage has been taken of conductive adhesives, which are of lower price than solders and enable the formation of ultra fine pitches with the potential to realize environmental friendly, fluxless and low temperature processes.

In spite of extensive research activities, flip chip technology using these environmental friendly ACF or ACP as connecting materials suffer from the disadvantage of being inefficient in production costs requiring many processes, including chip design and bump formation for ACA flip chip packaging, mass production of connecting materials, and automation of connecting processes. Therefore, wafer level flip chip package using ACA was developed to provide advantages in terms of production cost by simplifying the processes subsequent to the fabrication of conventional solder bump flip-chip packages[61-62].

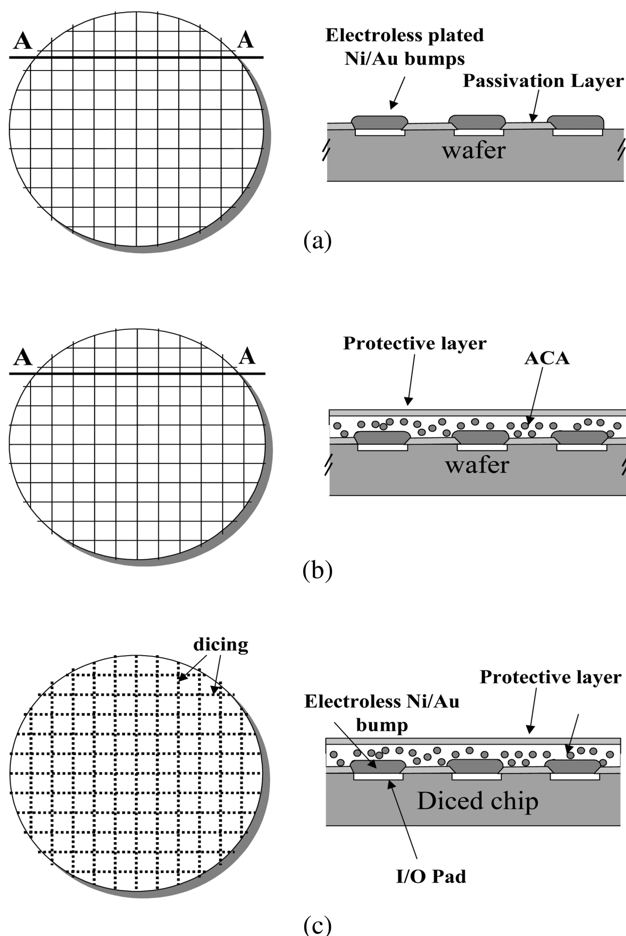


Fig. 14. (a) schematic views showing a wafer with non-solder bump formation and cross-section view along the line A-A'. (b) schematic views showing a wafer after ACA deposition on bump-formed wafer and its cross section view, (c) schematic views showing a dicing process and cross section of diced chip with ACA deposition.

Fabrication of wafer-level flip chip package using ACA comprised of forming a low priced non-solder bump on an I/O pad of each chip of a wafer, coating the ACA over the wafer, dicing the ACA coated wafer into individual chips by use of a wafer dicing machine, and subjecting the individual chips to flip-chip bonding as shown in Fig. 14. The application of ACA to the bump formed wafer can be achieved in a spraying, a doctor blade, or a meniscus coating process using ACP solution, and lamination of ACF. The film was laminated on the wafer in a thickness of 20-50 μm.

In wafer dicing process, the wafer with pre-applied ACA is mounted on a wafer dicing machine to confirm the scribe line of the wafer, after which the wafer is diced into individual chips. In this regard, ACA is required to be transparent and have such high adhesion as not to exhibit delamination during the process. After removing the protective layer from the diced chips, it is heat pressed against a circuit board so that the individual chips are electrically connected via the conductive particles of ACA onto the substrate pads. Wafer level flip chip package using ACA is economically favorable owing to its simplicity and environmental friendly process.

9. NCAs FOR LOW COST AND HIGH RELIABILITY

NCAs, basically materials composed of an adhesive polymer resin and curing agent, have brought much attention as an alternative of ACA for flip-chip-chip on organic boards due to the advantages of low cost and ultra-fine pitch capability[63-66]. For the full implementation of flip chip using NCAs, it is necessary to provide good reliability data to prove the availability of NCAs flip chip technology. The most commonly observed flip chip failure is occurred during the thermal cycling test, which is due to the thermal expansion mismatch between chips and substrates. Therefore, the problem of CTE mismatch between chips and substrates becomes serious with the NCAs flip chip assembly because of high CTE of NCAs materials without any filler. For this reason, novel NCAs that has low CTE for underfill-like function has been developed. Figure 15 shows the schematic draw of flip chip CSP using NCF as first level interconnection and its cross-section view of Au stud bump joint.

The addition of non-conducting silica filler of the NCA composite materials has control on the curing behavior, thermo-mechanical properties, and reliability for the NCA

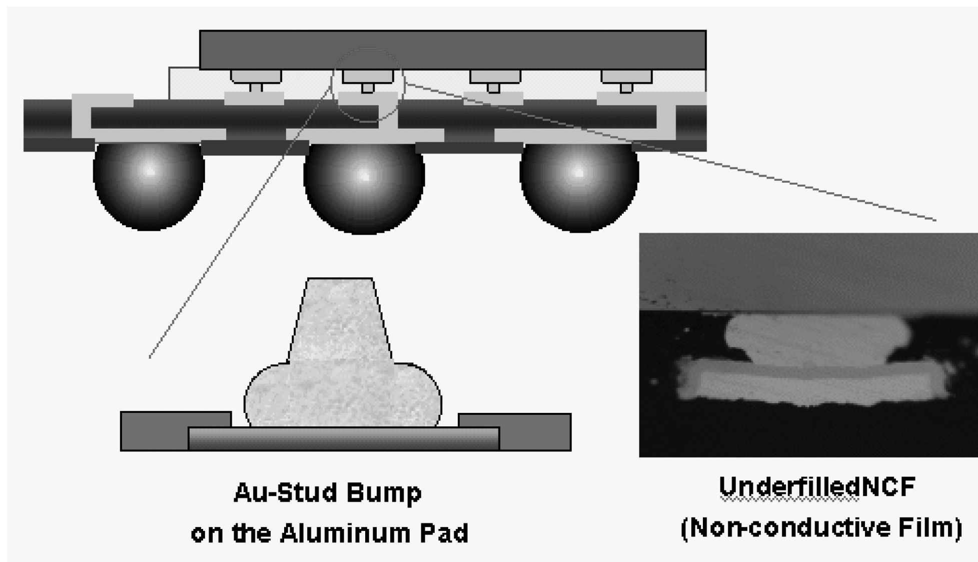


Fig. 15. Schematics of flip chip CSP using NCF and cross-section of NCF interconnection.

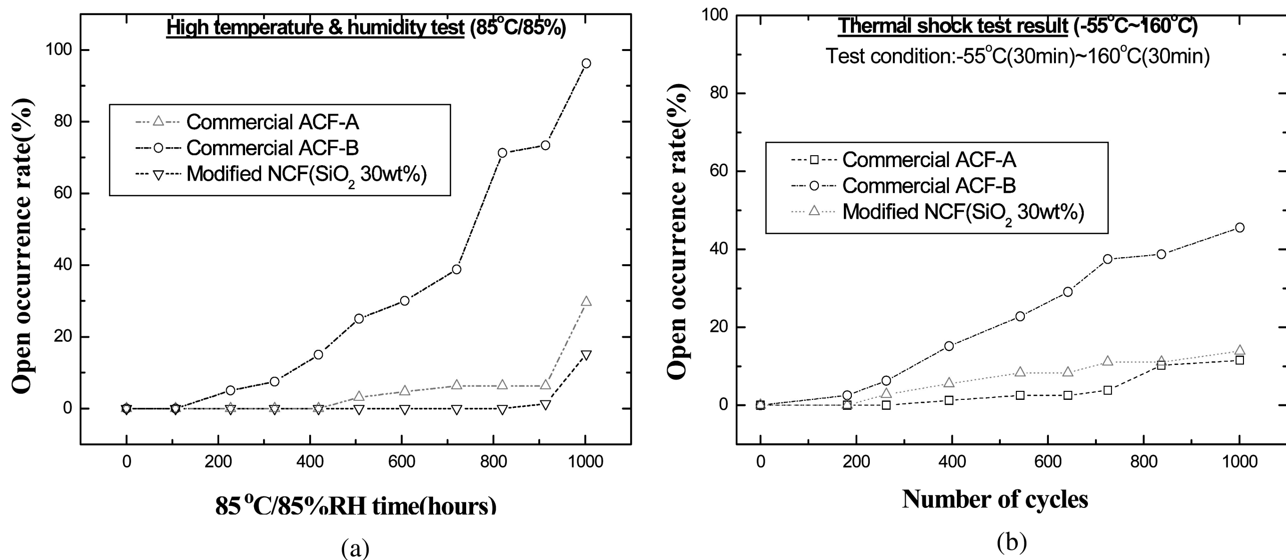


Fig. 16. Open occurrence rate of NCA flip chip interconnects (a) during 85 °C /85%RH test and (b) - 55°C ~ 160 °C thermal shock test.

flip chip assembly on an organic substrate. The content of non-conducting filler was optimized for the desirable thermo-mechanical properties of NCA composite materials such as proper curing profile, high Tg, low CTE and modulus, and strong adhesion. These effects of non-conducting filler addition on the NCA material properties were verified by reliability tests. The reliability of NCA flip chip assembly using modified NCA with non-conducting filler is significantly better than that of flip chip assembly using commercial ACF as shown in Fig. 16. Therefore, the incorporation of non-conductive fillers in the NCA composite material significantly improves the reliability of flip chip CSP using NCAs materials[67-68]. NCA materials continue to increase their applications with low cost, finer pitch interconnection, high reliability and processability. But the technical concerns for process and performance of NCAs such as high bonding pressure and electrical instability at high temperature should be resolved[69]. Recently, nano-sized metallic fillers are incorporated into NCA formulation for improved electrical and thermal conductivity, and reduced bonding pressure[70].

10. SUMMARY AND CONCLUSION

This paper described the recent development, research

works and applications of conductive adhesives as one of promising lead-free alternatives for electronic packaging and interconnection applications in terms of materials, process, and reliability concerns. Conductive adhesive materials have been evolved to meet the higher electrical/mechanical/thermal performance, fine pitch capability, low temperature process and strong adhesion/reliability requirements for electronic packaging module and assemblies. ICAs are becoming attractive in replacing SnPb or Pb-free solder alloys in die attach, SMT and flip chip assemblies with electrical, mechanical and reliability enhancements. More research works in improving those performances of ICAs together with material cost down are being pursued for electronics manufacturing without solder. ACAs, have been successfully used for fine pitch and Pb-free interconnection areas for flat panel displays and semiconductor packaging industries. New material systems for conductive fillers and adhesive matrix are being developed for ever-increasing demands of electrical, thermal, and reliability performances with fine-pitch, low temperature and fast cure ability, etc. Especially multi-layered ACF structures such as double and triple-layered ACFs for fine pitch COG and COF package technologies were developed, and underfil-like ACA/F and thermally conductive ACAs were developed for the reliable flip chip assembly under thermal cycling reliability and high current carrying reliability environments. High frequency characteristic of ACF flip chip interconnect was also investigated and found useful for RF and high frequency interconnect. Wafer level flip chip package using pre-applied ACF was demonstrated for wide use of ACF flip chip technology in mass production. For cost and ultra-fine pitch reasons, NCA/Fs are emerging materials as Pb-free & fine pitch conductive adhesive choices, and electrical performance and reliability enhancements were achieved through materials and process optimization. Research and developments for high performance and low cost conductive adhesives are in active stages.

Conductive adhesives and packaging technologies using them are expanding their applications and becoming great potential for Pb-free interconnection materials for electronic packaging applications.

REFERENCES

1. J. Liu ed., *Conductive Adhesives for Electronics Packaging*, E chap.1, Electrochemical Publications Ltd., British Isles (1999).
2. M. Zwolinski, J. Hickman, H. Rubin, Y. Zaks, S. McCarthy, T. Hanlon, P. Arrowsmith, and D. Napp, *IEEE Trans. Comp. Packag. Manufact. Technol.-Part. C* **19**, 241 (1996).
3. D. Lu and C. P. Wong, *IEEE Trans. Comp. Packag. Technol.* **23**, 620 (2000).
4. J. Liu, *Microsys. Technol*. **5**, 72 (1998).
5. J. C. Jagt, P. J. M. Beris, and G. F. C. M. Lijten, *IEEE Trans. Comp. Packag. Manufact. Technol.-Part. B* **18**, 292 (1995).
6. Y. Li and C. P. Wong, *Mater. Sci. and Eng. Report* **51**, 1 (2006).
7. I. Watanabe, Y. Gotoh, and K. Kobayashi, *Proc. Asia Display/IDW*, p. 553, Nagoya, Japan (2001).
8. H. Nishida, K. Sakamoto, and H. Ogawa, *IBM J. Research and Development*, **42**, 517 (1998).
9. D. J. Williams, D. C. Whalley, S. H. Mannan, and A. O. Ogunjimi, *Soldering & Surface Mount Tech.* **5**, 4 (1993).
10. J. Liu, A. Tolvgard, J. Malmodin, and Z. Lai, *IEEE Trans. Comp. Packag. Manufact. Technol.* **22**, 186 (1999).
11. P. Clot, J. F. Zeberli, J. M. Chenuz, F. Ferrando, and D. Styblo, *Proc. Electronics Manufact. Technol. Symp., 24th IEEE/CPMT.* p. 36, Austin, TX; IEEE (1999).
12. R. L. Dietz, D. Peck, P. J. Robinson, M. G. Firmstone, P. M. Bartholomew, and G. Paterson, *Soldering & Surface Mount Tech.* **9**, 55 (1997).
13. J. Miragliotta, R. C. Benson, T. E. Phillips, and J. A. Emerson, *Proc. Mater. Res. Soc. Symp*. **515**, 245 (1998).
14. D. Cavasin, K. Brice-Heams, and A. Arab, *Proc. 53rd Electronic Components and Technology Conf.* p. 1404, New Orleans, LO; IEEE (2003).
15. R. Kisiel, *J. Electron. Packag.* **124**, 367 (2002).
16. H. de Vries, J. van Delft, and K. Slob, *IEEE Trans. Comp. Packag. Technol.* **28**, 499 (2005).
17. K. Gilleo, *Enivironment-friendly Electronics: Lead-free Technology*, chap. 24, (ed. J. S. Hwang), Electrochemical Publications Ltd., Port Erin, UK (2001).
18. S. G. Hong and M. D. Ho, *J. Environmental Sci. Health. A.* **34**, 2043 (1999).
19. D. Lu and C. P. Wong, *Int. J. of Adhesion and Adhesives* **20**, 189 (2000).
20. D. Lu, Q. K. Tong, and C. P. Wong, *IEEE Trans. Comp. Packag. Technol.* **22**, 365 (1999).
21. Y. Li, A. Whitman, K. S. Moon, and C. P. Wong, *Proc. 55th Electr. Comp. and Technol. Conf.*, p.1648, Lake Buena Vista, FL (2005).
22. K. S. Moon, J. Wu, and C. P. Wong, *IEEE Trans. Comp. Packag. Technol.* **26**, 375 (2003).
23. S. K. Kang, S. Buchwalter, and C. Tsang, *J. Electron. Mater.* **29**, 1278 (2000).
24. Y. Li, K. S. Moon, and C. P. Wong, *IEEE Trans. Comp. Packag. Technol.* **29**, 173 (2006).
25. D. Lu, Q. K. Tong, and C. P. Wong, *IEEE Trans. Electr. Packag. Manufact.* **22**, 228 (1999).
26. D. Lu and C. P. Wong, *J. Appl. Polym. Sci.* **74**, 399 (1999).
27. H. Li, K. S. Moon, and C. P. Wong, *J. Electron. Mater.* **33**, 106 (2004).
28. D. Durad, D. Vieau, A. L. Chu, and T. S. Weiu, *US patent 5,180,523* (1989).
29. M. Hrovat, D. Belavic, and I. Hipot, *Electrotechnical Review* **58**, 93 (1991).

30. H. Schonhorn and L. H. Sharpe, *US Patent, 4,377,619* (1983).
31. H. Li, K. S. Moon, Y. Li, L. Fan, J. Xu, and C. P. Wong, *Proc. 54th Electronic Components and Technology Conf.* p.165, Las Vegas, NV; IEEE (2004).
32. W. S. Kwon, M. J. Yim, S. J. Ham, and K. W. Paik, *J. Electron. Packag.* **127**, 86 (2005).
33. R. Joshi, *Microelectr. Journal.* **29**, 343 (1998).
34. I. Watanabe, K. Takemura, N. Shiozawa, and T. Ohta, *Flip Chip Technologies*, (ed. John H. Lan) pp. 301-315, McGraw Hill (1996).
35. M. J. Yim, J. S. Hwang, and K. W. Paik, *Int'l J. of Adhesion and Adhesives* (in press).
36. J. Tjandra, C. L. Wong, J. How, S. Peana, M. Mita, and G. Murakami, *Proc. Electr. Packag. Technol. Conf., EPTC*. p. 52, Singapore, IEEE/CPMT (1997).
37. Y. Kumano, Y. Tomura, M. Itagaki, and Y. Bessho, *Microelect. Reliab.* **41**, 525 (2001).
38. S. M. Chang, J. H. Jou, A. Hsieh, T. H. Chen, C. Y. Chang, Y. H. Wang, and C. M. Huang, *Microelect. Reliab.* **41**, 2001 (2001).
39. R. Aschenbrenner, J. Gwiasda, J. Eldring, E. Zakel, and H. Reichl, *Int. J. Microcir. and Elect. Packag.* **18**, 154 (1995).
40. M. J. Yim, J. S. Hwang, J. G. Kim, J. Y. Ahn, H. J. Kim, W. S. Kwon, and K. W. Paik, *J. Electron. Mater.* **33**, 76 (2004).
41. R. Miessner, R. Aschenbrenner, and H. Reichl, *Proc. 49nd Electronic Components and Technology Conf.,* p. 595, San Diego, CA; IEEE (1999).
42. G. Sarkar, S. Mridha, T. T. Chong, W. Y. Tuck, and S. C. Kwan, *J. Mater. Proc. Technol.* **89**, 484 (1999).
43. J. Liu and Z. Lai, *J. Electron. Packag.* **124**, 240 (2002).
44. M. J. Yim and K. W. Paik, *IEEE Trans. Comp. Packag. Manufact. Technol.* **24**, 24 (2001).
45. C. Y. Yin, H. Lu, C. Bailey, and Y. C. Chan, *Soldering and Surf. Mount Technol.* **18**, 27 (2006).
46. C. Yin, H. Lu, C. Bailey, and Y. C. Chan, *Circuit World.* **111**, 20 (2005).
47. C. Yin, H. Lu, C. Bailey, and Y. C. Chan, *IEEE Trans. Electr. Packag. Manufact.* **27**, 254 (2004).
48. L. Cao, Z. Lai, and J. Liu, *J. Elec. Packag.* **127**, 43 (2005).
49. M. J. Rizvi, Y. C. Chan, C. Bailey, H. Lu, and A. Sharif, *Soldering & Surf. Mount Tech.* **17**, 40 (2005).
50. K. K. Lee, N. H. Yeung, and Y. C. Chan, *Soldering & Surf. Mount Tech.* **17**, 4 (2005).
51. M. J. Yim, W. H. Ryu, Y. D. Jeon, J. H. Lee, S. Y. Ahn, J. H. Kim, and K. W. Paik, *IEEE Trans. Comp. Packag. Manufact. Technol.* **22**, 575 (1999).
52. R. Sihlbom, M. Dernevik, Z. Lai, J. P. Starski, and J. Liu, *IEEE Trans. Comp. Packag. Manufact. Technol.* **21**, 469 (1998).
53. G. Dou, Y. C. Chan, J. E. Morris, and D. C. Whalley, *Soldering and Surf. Mount Technol.* **18**, 3 (2006).
54. M. J. Yim, I. H. Jeong, H. K. Choi, J. S. Hwang, J. Y. Ahn, W. S. Kwon, and K. W. Paik, *IEEE Trans. Comp. Packag. Technol.* **28**, 789 (2005).
55. S. H. Fan and Y. C. Chan, *J. Electron. Mater.* **32**, 102 (2003).
56. M. J. Yim, H. J. Kim, and K. W. Paik, *J. Electron. Mater.* **34**, 1165 (2005).
57. H. J. Kim, W. S. Kwon, and K. W. Paik, *Proc. 5th Int'l Conference on Electronic Materials and Packaging,* p. 203, Singapore (2003).
58. J. Haberland, B. Pahl, S. Schmitz, C. Kallmayer, R. Aschenbrenner, and H. Reichl, *Proc. 52nd Electronic Components and Technology Conf.,* p.144, San Diego, CA (2002).
59. P. Garrou, *IEEE Trans. on Adv. Packag.* **23**, 198 (2000).
60. Q. Tong, B. Ma, S. Hong, L. Nguyen, H. Nguyen, and A. Negasi, *Proc. 52nd Electronic Components and Technology Conf.,* p.1366, San Diego, CA (2002).
61. K. W. Paik and M. J. Yim, *US Patent 6,518,097* (2003).
62. H. Y. Son, C. K. Chung, M. J. Yim, and K. W. Paik, Proc. *56th Electr. Comp. and Technol. Conf.,* p.565, San Diego, CA (2006).
63. H. Yu, S. G. Mhaisalkar, E. H. Wong, L. K. Teh, and C. C. Wong, *IEEE Trans. Comp. Packag. Technol.* **29**, 71 (2006).
64. W. K. Chiang, Y. C. Chan, B. Ralph, and A. Holland, *J. Electron. Mater.* **35**, 443 (2006).
65. Z. W. Zhong, *J. Electron. Packag.* **127**, 29 (2005).
66. L. K. Teh, C. C. Wong, S. Mhaisalkar, K. Ong, P. S. Teo, and E. H. Wong, *J. Electron. Mater.* **33**, 271 (2004).
67. M. J. Yim, J. S. Hwang, W. S. Kwon, K. W. Jang, and K. W. Paik, *IEEE Trans. Electr. Packag. Manufact.* **26**, 150 (2003).
68. K. W. Paik and M. J. Yim, *US Patent 6,930,399* (2005).
69. H. C. Cheng, C. L. Ho, K. N. Chiang, and S. M. Chang, *IEEE Trans. Comp. Packag. Technol.* **27**, 398 (2004).
70. Y. Li, K. S. Moon, and C. P. Wong, *J. Electron. Mater.* **34**, 1573 (2005).