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Chip-underfill Interfaces of Flip Chip Plastic Ball Grid Array Packages

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High performance electronic packages sometimes fail due to interfacial adhesion degradation during reliability tests. A chip is placed onto a laminate chip carrier in the case of flip chip plastic ball grid array (FC-PBGA) packages. When a flux with pimelic acid is used in a flip chip joining process of a FC-PBGA, it reacts with SnO and SnO_2 on chip solder balls or the eutectic paste of the laminate to yield organotin compounds including tin pimelate. There is also minor residue such as tin oxides. The flux residue deposits onto polyimide (PI) which is the passivation layer of integrated circuit chips. In order to improve the reliability of such packages, underfill is introduced into the gap between chip and laminate. The reliability of the underfilled module is tested by subjecting to JEDEC preconditioning at 30 deg.C and 60% relative humidity followed by a solder reflow process at 220-260 deg.C. C-mode scanning acoustic microscopy (CSAM) on such modules shows some delaminated areas at the chip-underfill interface. It is proposed that JEDEC preconditioning of an FC-PBGA package introduces water molecules that accumulate at the flux residue-underfill interface. The interactions between the PI surface and the underfill are broken. Thus, the interface is weakened. Various types of mechanical stresses, which increase during subsequent solder reflow, cause the weakened interfaces to delaminate.

Key words: interface, adhesion, reliability, electronic, package, reflow.

1. INTRODUCTION

A typical flip chip plastic ball grid array (FC-PBGA) package consists of BGAs, a laminate with solder mask, solder joints, a chip and a lid as shown in Fig. 1. The major components of a laminate are polymer, inorganic filler and copper circuitry while the major component of a chip is silicon. The coefficient of thermal expansion of a laminate (11-17 $\times 10^{-6}$/°C) is greater than that of a chip (2.6×10^{-6}/°C) [1]. Mismatch of the thermal expansion between the laminate and the chip leads to the build up of stresses that can cause cracks at the C4 solder joints in reliability tests involving temperature, humidity, and thermal cycling. Thus, an FC-PBGA package typically requires an underfill material to keep moisture away from solder interconnections and to reinforce the solder joints which are prone to fatigue.

As the number of transistors increase in modern high performance microelectronic devices, densities of wiring and solder balls in chips increase as does the size of a chip. As the size of a chip increases, so does the stress at the chip-laminate interface. Durable adhesion is one of the most important considerations in employing an underfill material which must adhere to the passivation layer at the chip side as well as to the solder mask at the laminate side in order to be effective. Here we report on the adhesion failure at the polyimide-underfill interface of a high performance package.

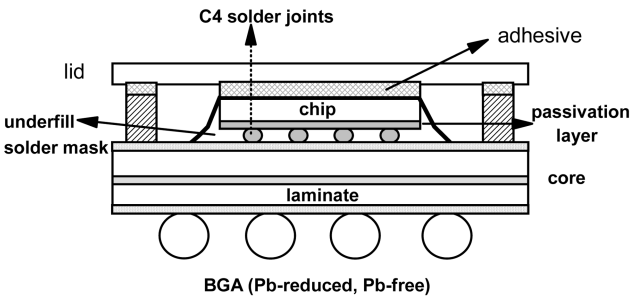

Fig. 1. Schematic cross-section of a typical FC-PBGA package.

2. RESULTS AND DISCUSSION

2.1. Chip-Underfill Delamination and Failure Mode

A flux containing pimelic acid and organic solvents was dispensed onto a laminate and then a chip was placed. This laminate/chip sample went through a reflow process using an oven at 220-265 °C for 2-3 min. Underfill was applied

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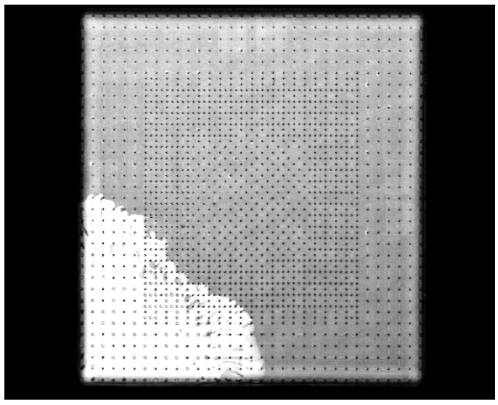


Fig. 2. CSAM image of a module with a chip and a laminate. White spots correspond to delaminated areas.

into the gap between the chip and the laminate followed by curing in an oven at 150 °C for 30 min.

In order to ensure module package integrity and function after BGA solder attach to a card or board, JEDEC preconditioning is required. It includes three steps: (1) baking at 125 °C for 24 h, (2) moisture soak, and (3) solder reflow at 220 - 265 °C three times. The reflow process simulates module attachment to a printed circuit card or board. For conventional eutectic solder (Pb/Sn = 37/63) attachment, a typical reflow temperature is 220 °C. However, environmental concerns require lead elimination and the replacement with lead-free solder alloys requires a higher reflow temperature in the range of 245 - 265 °C.

To detect voids and delamination in FC-PBGA packages, C-mode scanning acoustic microscopy (CSAM) is employed. Scanning acoustic microscopy is a non-destructive imaging technique whereby ultrasonic pulses are transmitted via a transducer into a sample at a predetermined focal plane. The acoustic medium between a transducer and a sample is deionized (DI) water. As the transducer traverses the sample, the reflected acoustic signals are collected by the receiver and processed digitally. A gating system allows operators to identify selectively which portion of the received signal to display for analysis. The transmit-receive-gate-display process is replicated hundreds of times as the transducer is passed over a sample. Voids and delamination that alter the normal acoustic signal are typically displayed as bright areas while intact materials are shown as dark areas. Figure 2 shows the CSAM image of the prepared package mentioned above. There is a massive delamination at the bottom left corner of the chip.

The cross-section of a delaminated region shows a small gap between the polyimide passivation layer and the underfill as shown in Fig. 3. To further understand why and how such delamination occurred and to study the locus of failure at the nano-scale, a chip was separated from the underfill and laminate part in a module and then X-ray photoelectron

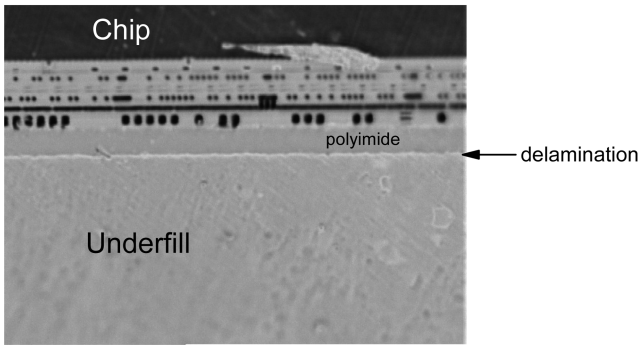


Fig. 3. SEM picture on the cross-section of a delaminated region.

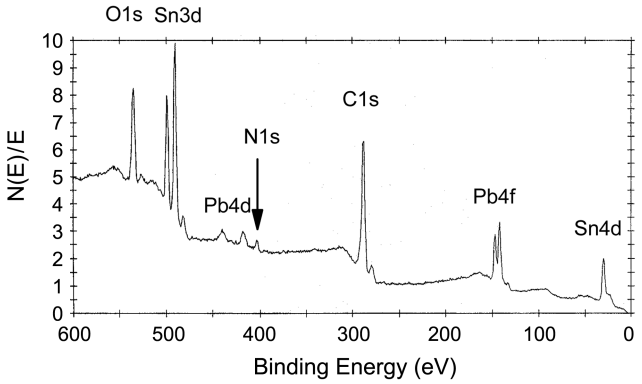


Fig. 4. XPS spectrum of the chip side after separating the underfill/laminate side in the delaminated region of a module shown in CSAM.

spectroscopy (XPS) was conducted on the chip and underfill sides corresponding to the delaminated (white) areas in CSAM.

A typical XPS survey spectrum on the chip side is shown in Fig. 4. The spectrum shows the relatively intense Sn_{3d} bands at 490 eV and the weak N_{1s} band at 401 eV. This result indicates that the PI surface is covered with a thin layer of organotin compounds and that the failure occurs at the interface between the organotin compounds and the underfill.

2.2. Model Study for Formation of Flux Residue in Chip Joining

To understand the reaction of tin oxide with the flux that contains pimelic acid, tin foil with surface tin oxide was cut into small pieces (approximately 1.0 mm or smaller). The flux was dispensed onto a PI-coated stainless steel cap (12.5 mm × 17.0 mm) or a piece of PI-coated silicon wafer (12.5 mm × 25.0 mm). Then small pieces of tin foil were placed on the flux/PI substrate. These samples were heated on a hot plate to 120 °C for 10 min to allow reaction of pimelic acid with tin oxide. A white residue formed on the PI. The tin foil was removed to avoid melting at the reflow temperature. Samples were then heated on a hot plate under nitrogen to

245 °C and held for 5 min. Some white residue was still visible on approximately half of the substrate surface. The white residue was analyzed with XPS. The XPS survey spectrum in Fig. 5 exhibits intense bands of C_{1s}, O_{1s} and Sn_{3d} due to the residue as well as a weak N_{1s} band due to PI, indicating that the PI surface is covered with a thin layer of compounds containing the elements of C, O, and Sn. These are likely the same organotin compounds as those found in a delaminated package.

Reflection absorption infrared (RAS-IR) spectroscopy was employed to understand the reaction of flux with tin oxide at the molecular level. Cr (100 nm), a reflective metal, was sputter-coated onto a silicon wafer followed by indium-tin-oxide (ITO, 50 nm). As shown in Fig. 6, ITO did not react with the flux at 120 °C. Heating at 245 °C did not leave any residue on ITO.

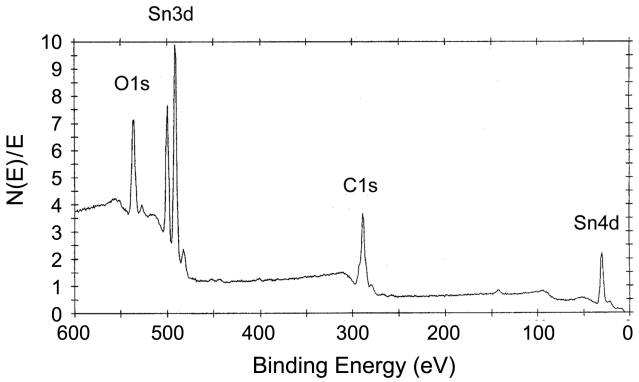


Fig. 5. XPS survey spectrum.

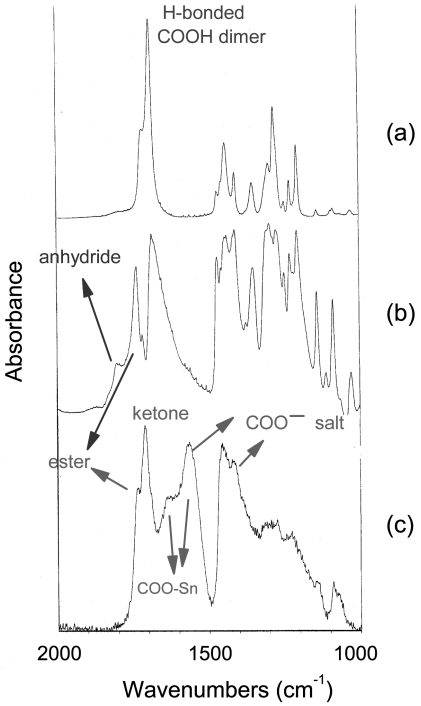
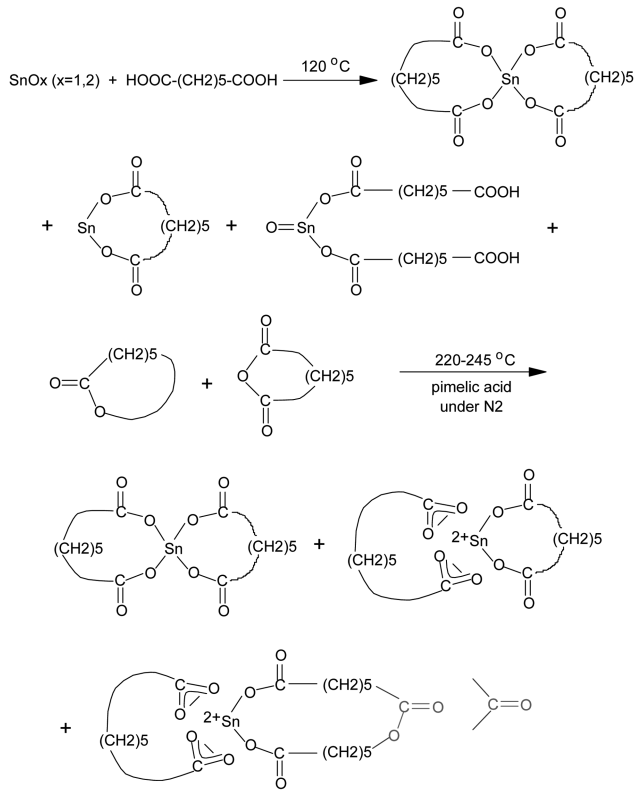


Fig. 6. RAS-IR spectra of the reaction products between pimelic acid and SnO_2. (a) Control experiment of heating only the flux at 120 °C for 10 min, (b) reaction of pimelic acid with SnO and SnO_2 (pieces of tin foil) at 120 °C for 10 min, and (c) removed the pieces of tin foil after the process described in (b), and then heated the white residue at 245 °C for 5 min.

The flux consists of pimelic acid and solvent. After evaporating the solvent at 120 °C, solid pimelic acid remained on the ITO. Figure 6(a) shows the RAS-IR spectrum of pimelic acid, [HOOC-$(CH_2)_5$-COOH]. The pattern of the spectrum is very similar to that of the transmittance spectrum for pimelic acid. The spectrum in Fig. 6(a) displays two peaks at 1715 and 1688 cm^{-1} which usually correspond to the carbonyl stretching of hydrogen bonded carboxylic acids. The RAS-IR spectra in Figs 6(b) and 6(c) display the peaks corresponding to ester (1735 cm^{-1}), ketone (1711 cm^{-1}) and carboxylate salt (1422, 1454, 1564 cm^{-1}), suggesting that tin pimelate ester, tin pimelate salt, ketone, and ester are the major functional groups of the reaction products. A peak (1799 cm^{-1}) due to anhydride appeared in Fig. 6(b) and disappeared in Fig. 6(c), indicating that an anhydride compound(s) was formed at 120 °C and then decomposed at 245 °C. This reaction is expected since two COOH groups of pimelic acid easily form an anhydride compound which decomposes subsequently at high temperature to CO_2 and cyclic ketone. The oxidation state of Sn at the surface of solder balls and tin foil should be IV instead of II since Sn (IV)



Scheme 1. Proposed reactions of pimelic acid with SnOx (x=1, 2) on the basis of the XPS and RAS-IR data.

oxide is more stable than Sn (II) oxide and tin (IV) acetate is more stable than tin (II) acetate[2]. It is also understood that the first surface layer of Sn metal is tin (IV) oxide and the next layer is tin (II) oxide. On the basis of the RAS-IR spectra and the previously discussed XPS data, the reaction of pimelic acid with SnO and SnO_2 is proposed as shown in Scheme 1.

2.3. Formation of Flux Residue on Real Chips

On the basis of the experimental result for the reaction between a flux of pimelic acid and SnO_x ($x = 1, 2$), it can be anticipated that the flux also reacts with SnO_x on solder balls of a chip and solder paste on laminate pads to produce thermally stable organotin compounds and to subsequently deposit these onto the PI surface. The flux (10 μl) was placed on a blanket laminate without metallic pads and then a chip with Pb/Sn solder balls was placed on the laminate and clipped together. The sample went through the reflow process under nitrogen at 245 ^{o}C in an oven. After separating the laminate, the chip surface was analyzed with a microscope and XPS. Some residue can be seen even with a microscope (Fig. 7) and the XPS spectrum showed strong Sn_{3d} and C_{1s} bands, indicating that organotin compounds were formed.

3. SUMMARY

Pimelic acid, an active ingredient of the flux employed in this study, reacts with SnO and SnO_2 on solder balls of chips and/or eutectic paste applied on laminates to leave a thermally stable residue on the polyimide chip-passivation layer. The major components of this flux residue are organotin compounds. The organotin compounds on PI, when not cleaned, cause delamination usually at the underfill-chip interface, specifically at the underfill-flux residue (organotin) interface. Removal of the organotin residue prior to underfill application enhances the chip-underfill adhesion.

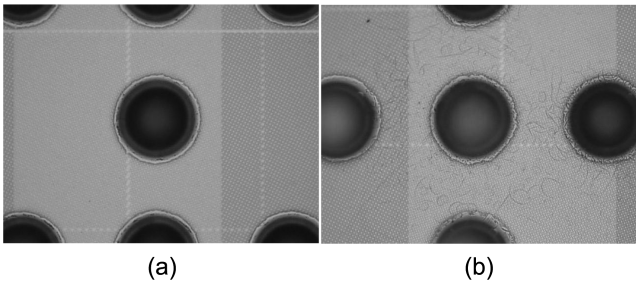


Fig. 7. Microscope pictures of chips. (a) Untreated and (b) treated with the flux of pimelic acid and then reflowed. The large black closed circles are solder balls and the yellowish area is the PI passivation layer. The fibers around the solder balls in (b) are flux residue.

REFERENCES

1. R. R. Tummala and E. J. Rymaszewski, *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York, NY (1989).
2. F. A. Cotton and G.Wilkinson, *Advanced Inorganic Chemistry*, John Wiley & Sons, New York, NY (1972).