

High Frequency Properties of Anisotropic Conductive Films (ACFs) for Flip Chip Package Application

Myung Jin Yim and Kyung Wook Paik*

Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology
373-1, Guseong-dong, Yuseong, Daejeon 305-701, Korea

In this paper, the high frequency properties of anisotropic conductive films (ACFs) in flip chip interconnects at the RF and high-frequency range were investigated. To evaluate the high frequency model parameters, which are based on an ACF flip chip model and a network analysis, high-frequency measurements of test flip chip vehicles that used different bonding materials were evaluated. Furthermore, to demonstrate real applications for an ACF interconnection at the RF and high-frequency range, ACF flip chip technologies were applied to assemble a passive device that uses an RF integrated passive device, and also, an active device that uses a highly integrated monolithic microwave integrated circuit device on an RF module. Furthermore, the high-frequency characteristics of these devices with those of flip chip assemblies fabricated via conventional methods such as solder ball interconnection were compared.

Keywords: flip chip, anisotropic conductive films, high-frequency, Pb-free, electronic packaging

1. INTRODUCTION

Recently, demand within the electronics industry for wireless communications and radar systems with fully-integrated RF devices in the broadband operational range is increasing. The performance of high-speed devices and systems is limited by discontinuity of package interconnects, which are influenced by the geometry, material, and joint mechanism of package interconnects. For the first level package technology between a chip and a substrate, three bonding technologies are generally available: wire bonding, tape automated bonding, and flip chip bonding.

Flip chip technology meets today's packaging needs of semiconductors and high-speed devices, especially with respect to miniaturizing packages and reducing interconnection distances for a high standard of performance in RF and high-frequency applications. Numerous alternative interconnection methods that use a variety of materials such as solder, gold, and conductive adhesive are employed to make flip chip assemblies. Thus far, the use of solder balls has been the preferred method of assembling flip chips. However, the use of conductive adhesives, such as isotropic conductive adhesives and anisotropic conductive adhesives (ACAs), is attracting considerable attention as an alternative to solder because it overcomes the problem of solder bumps^[1-3]. Moreover, anisotropic conductive adhesives have the following

advantages: lower processing temperature (that is, the epoxy curing temperature is less than 150 °C, whereas the solder reflowing temperature is 240 °C); a finer pitch interconnect (less than 50 μm); lower cost due to fewer processing steps; and a green or Pb-free process (with no lead, fluxes, or cleaning solvents). In particular, flip chip assemblies that use anisotropic conductive film (ACF) have already been successfully implemented in low-cost, mass production of reliable assemblies such as chip-on-glass, chip-on-film, and chip-on-board assemblies^[4-6].

This trend is expected to continue for high-frequency applications where flip chip interconnection methods must have low cost, a high level of reliability, and a fine-pitch. These methods are necessary, for example, in RF ICs, RF ID tags, RF integrated passive devices (IPD), and fast memories in some packaged flip chips and direct chip attachments.

While investigating the high-frequency characteristics of flip chip interconnects that use ACF, we focused on bump metallurgy and the material properties of ACF. We also evaluated the electrical performance of an ACF flip chip package in the RF and high-frequency range by demonstrating flip chip assemblies that use real ICs of RF monolithic microwave integrated circuits (MMICs) and RF IPDs.

2. EXPERIMENT

2.1. Preparation of ACF Material

For reliable flip chip assembly in high-frequency applica-

*Corresponding author: kwpaik@kaist.ac.kr

tions, ACFs should have material properties such as lower coefficient of thermal expansion (CTE), higher modulus, and lower dielectric constant^[7]. We prepared two ACF materials, one containing only conductive fillers, the other conductive and nonconductive fillers. The conductive filler was made of Ni particles with a diameter of 5 μm and a content of 10 wt%; the nonconductive filler was made of an SiO_2 filler with a diameter of 0.8 μm and a content of 30 wt%. The nonconductive SiO_2 filler was added to a conventional ACF formulation to investigate the dielectric property of the ACF resin system and its effect on the high-frequency performance of flip chip interconnects that use ACF. To prepare the ACF resin solution, an homogenous mixing process of liquid epoxy, solid epoxy, curing agent, fillers and solvent, antioxidant agents, and coupling agents were added. And then ACFs were fabricated using a coating process on the release film, followed by a slitting process.

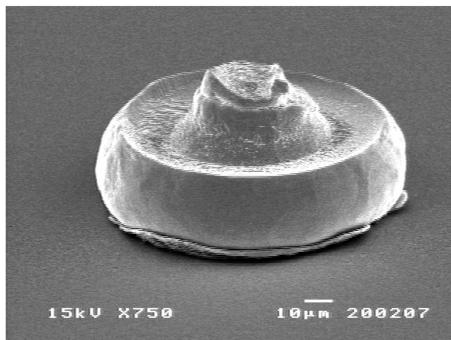
Next, the cured ACF samples were prepared by placing the adhesive mixture in a convection oven at 150 $^\circ\text{C}$ for 30 min. And then the samples were cut to a thickness of 0.6 mm for thermomechanical characterization through dynamic mechanical and thermomechanical analyses (TMA). The dielectric properties of the ACF samples were measured in a high frequency range of 10 MHz to 1.8 GHz. The samples

for measuring the AC dielectric properties were disc-shaped, and an Au evaporation method was used to prepare both electrodes of the samples.

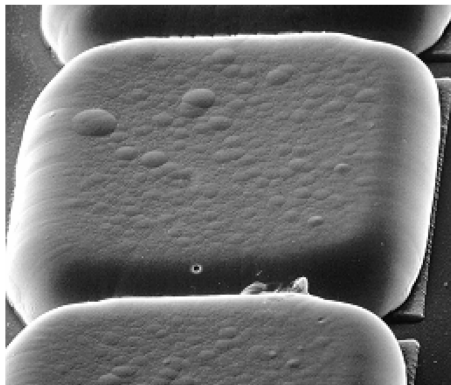
2.2. Flip Chip Assembly with ACF and High-Frequency Characterization

For the bumps on the I/Os of a test chip, Au stud bumps and electroless Ni/Au bumps were prepared. First, a modified wire bonding machine was used to form the gold stud bumps, with a height of 60 μm height and a diameter of 80 μm on each I/O pad of the test chips. As shown in Fig. 1-(a), each bump has an acute tail to provide good metal-to-metal contact during thermo-compression bonding with the ACF. Fig. 1(b) shows 20 μm electroless Ni/Au bumps that formed on each I/O of the chip by means of electroless plating.

Figure 2 shows the steps of the bonding process for the flip chip assemblies that use ACF materials. First, the ACF was attached onto the substrate and then the release film was removed, after which the bumps were aligned on the chip and the I/O pads on the substrates. Finally, for the thermo-compression bonding, bonding parameters of 100 MPa pressure and 180 $^\circ\text{C}$ temperature was employed for 20 seconds. Thus, the chip was electrically connected to the substrate pad via conductive particles or via direct contact with the bumps on the substrate pad, and then ACF resin was cured to mechanically adhere the chip to the substrate.



(a)



(b)

Fig. 1. Scanning electron microscopy images of (a) Au stud bumps and (b) electroless Ni/Au bumps formed on Al pads of test chip.

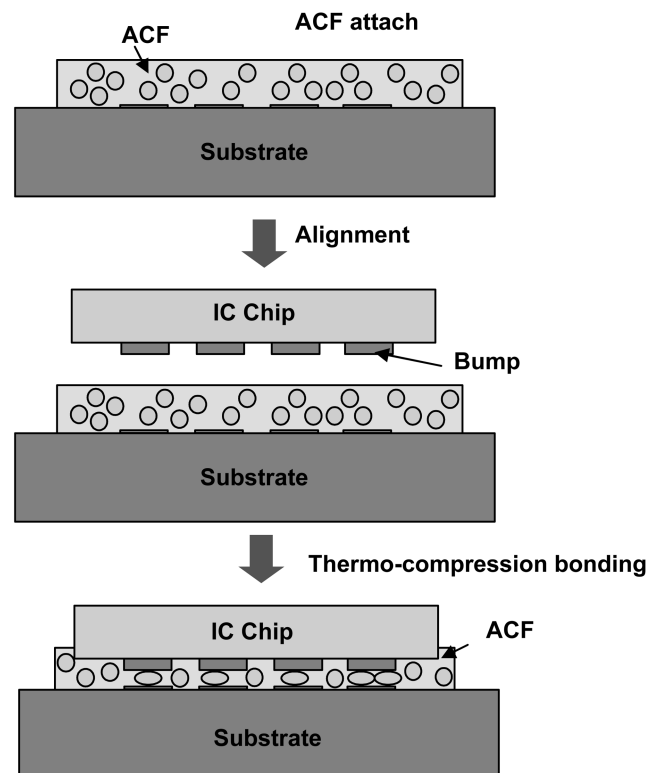


Fig. 2. Schematic of flip chip bonding process using ACF.

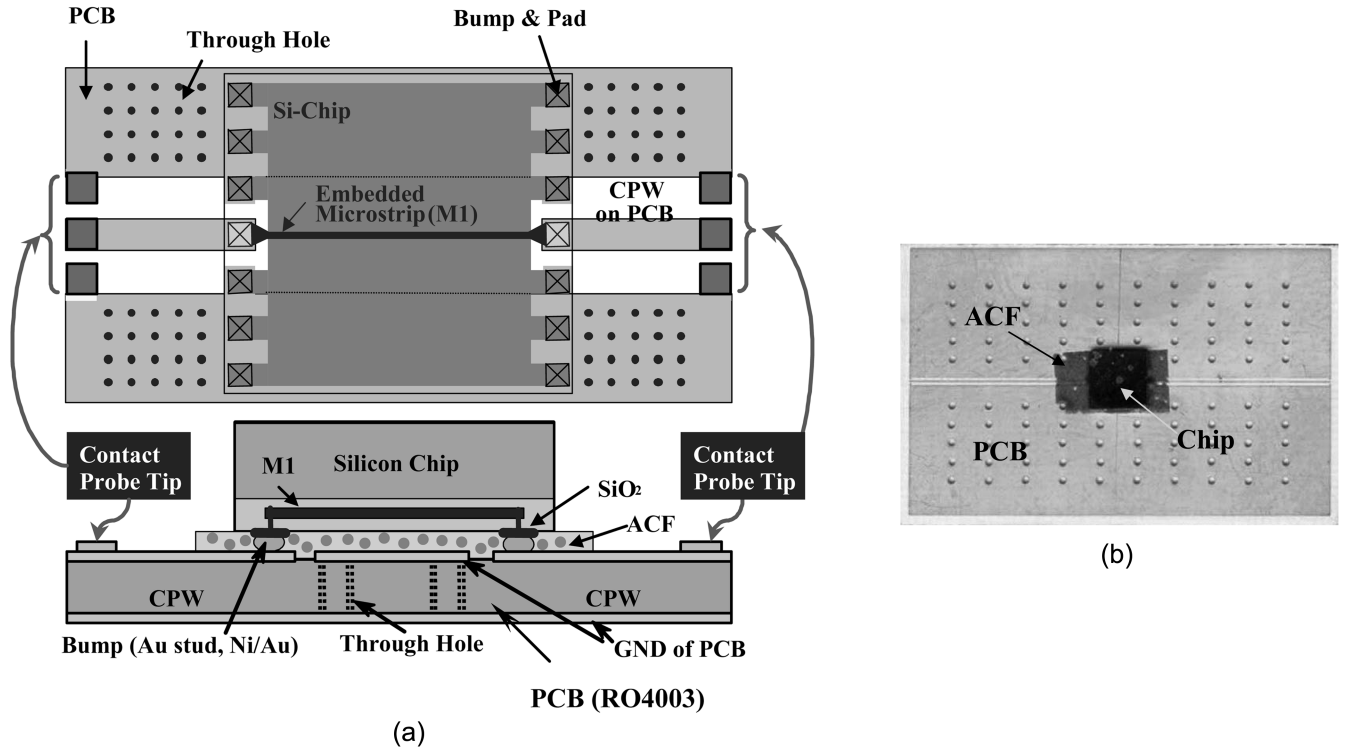


Fig. 3. (a) Schematic and (b) photograph of the device under testing for high frequency characterization of flip chip interconnect with ACF.

In order to investigate how the dielectric property of ACF affects the impedance parameters of a flip chip interconnect with a Ni/Au-bumped chip, two kinds of ACF with a different dielectric constant were used as interconnection materials; first, a conventional ACF, containing only conductive Ni particles and second a low-k ACF, containing conductive Ni particles and dielectric SiO₂ particles, as described in section 2-1. Moreover, for the test vehicle used to investigate how the bump system affects the impedance parameters of ACF flip chip interconnects, we used test chips with two different bumps, Au studs and electroless Ni/Au bumps. In this case, the conventional ACF containing only Ni particles was used.

In order to measure the high-frequency characteristics of an ACF flip-chip interconnect, a test method based on previous studies was used to extract the impedance parameters of the interconnects^[8, 9]. A test chip with a 20 μm width microstrip and a 3.3 mm×3.3 mm chip area was fabricated using a 1-poly and 3-metal 0.6 μm Si process. And then the microstrip with an inverted, embedded microstrip structure was fabricated to minimize the parasitic effect due to orientation and ground impedance. Figure 3 shows a schematic and photograph of the device.

To measure the S-parameters and to extract the impedance parameters of the ACF flip chip interconnects, an HP8510C vector network analyzer and a Cascade's probe system in a frequency range of 200 MHz to 20 GHz^[9] were used. After measuring the S-parameters of the test chip, the test PCB,

and the flip chip bonded device, a microwave network analysis was conducted to investigate the impedance parameter model of the ACF flip chip interconnect. Figure 4 shows the procedure used to extract the impedance parameters. The total ABCD parameters of the measurement can be easily determined from the measured S-parameters, as shown in the following equations:

$$A = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \quad (1)$$

$$B = Z_o \frac{(1 + S_{11})(1 - S_{22}) - S_{12}S_{21}}{2S_{21}} \quad (2)$$

$$C = \frac{1}{Z_o} \frac{(1 + S_{11})(1 - S_{22}) - S_{12}S_{21}}{2S_{21}} \quad (3)$$

$$D = \frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{2S_{21}} \quad (4)$$

Then, to calculate the de-embedded Z₁ and Z₂ parameters of the stud bump interconnects, we used the extracted ABCD parameters of the total test chip (A_T, B_T, C_T, and D_T), the CPW on the PCB (A_p, B_p, C_p, and D_p), and the line of the inverted embedded microstrip on the silicon substrate (A_o, B_o, C_o and D_o). Assuming negligible ground impedance and quasi-TEM wave transmission through the microstrip line, we then performed a Cascade transmission matrix conversion to determine impedance the Z₁ and Z₂ impedance as follows:

$$\begin{bmatrix} A_{p1} & B_{p1} \\ C_{p1} & D_{p1} \end{bmatrix}^{-1} \begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} \begin{bmatrix} A_{p2} & B_{p2} \\ C_{p2} & D_{p2} \end{bmatrix}^{-1} = \begin{bmatrix} 1 & Z_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} A_o & B \\ C_o & D_o \end{bmatrix} \begin{bmatrix} 1 & Z_2 \\ 0 & 1 \end{bmatrix} \quad (5)$$

Finally, by assuming reciprocity of the microwave network analysis, the stud bump interconnection impedance of Z_1 and Z_2 were calculated as follows:

$$Z_1 = \frac{1}{C_o} [K_{p1} K_{p2} \{D_{p2}(D_{p1} A_T - B_{p1} C_T) - C_{p2}(D_{p1} B_T - B_{p1} D_T)\} - A_o] \quad (6)$$

$$Z_2 = \frac{1}{C_o} [K_{p1} K_{p2} \{A_{p2}(A_{p1} D_T - C_{p1} B_T) - B_{p2}(A_{p1} C_T - C_{p1} A_T)\} - D_o] \quad (7)$$

Consequently, the high-frequency transmission characteristics of the ACF flip chip interconnect were successfully acquired.

2.3. ACF Flip Chip Assemblies by a Functional IC

2.3.1. Flip chip assembly for RF IPDs

An RF IPD on an organic substrate was assembled by using an electroless Ni/Au bump and the ACF flip chip method to produce a flip chip assembly that uses real functional ICs in the RF and high-frequency range. For the RF IPDs, the Telephus 900 MHz and 1800 MHz lumped low pass filters with dimensions of $0.9 \text{ mm} \times 0.9 \text{ mm}$ and a thickness of 0.6 mm were used. We fabricated the filters on thick oxide wafers using a $10 \text{ }\mu\text{m}$ Cu plating process with benzocyclobutene passivation^[10]. A FR-4 organic substrate with a dielectric constant (ϵ_r) of 4.8 and a thickness of 1 mm was employed. And then the insertion loss behavior of the ACF flip chip interconnect in the range of 500 MHz to 3.5 GHz was evaluated. In order to compare the RF performance, solder bumps were used to evaluate the flip chip interconnects with the same low pass filters. The solder bumps were eutectic Pb/Sn solder $300 \text{ }\mu\text{m}$ in diameter and $3 \text{ }\mu\text{m}$ thick electroless Ni/Au under bump metallization.

2.3.2. Flip chip assembly for RF MMICs

An RF MMIC was assembled on a glass substrate by using an Au stud bump and the ACF flip chip method so as to demonstrate the high standard of performance and simple fabrication process of an RF MMIC package. For the RF MMIC, a $0.5 \text{ }\mu\text{m}$ low noise E/D GaAs MESFET process was used to fabricate a low noise amplifier (LNA) chip for a PCS CDMA application. And a soda-lime glass substrate was also used with a thickness of 1 mm and ϵ_r of 4.0, and Au metallization was patterned on the substrate to a thickness of $0.2 \text{ }\mu\text{m}$. First, an LNA chip was bonded on the patterned glass substrate with ACF, and then matching passive components were assembled on the same substrate with an Ag paste. The noise and gain properties were then measured in the range of 1.7 GHz to 2.1 GHz with a test module configuration on glass.

3. RESULTS AND DISCUSSION

3.1. Material Characterization

3.1.1. CTE measurements of ACFs

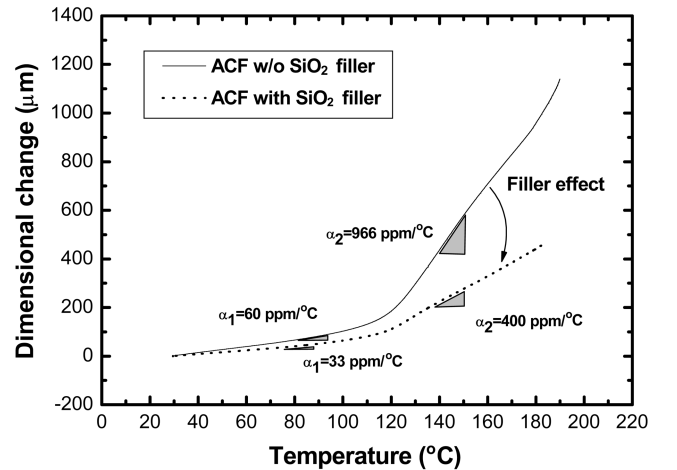


Fig. 5. TMA curves of ACFs samples with different content fillers.

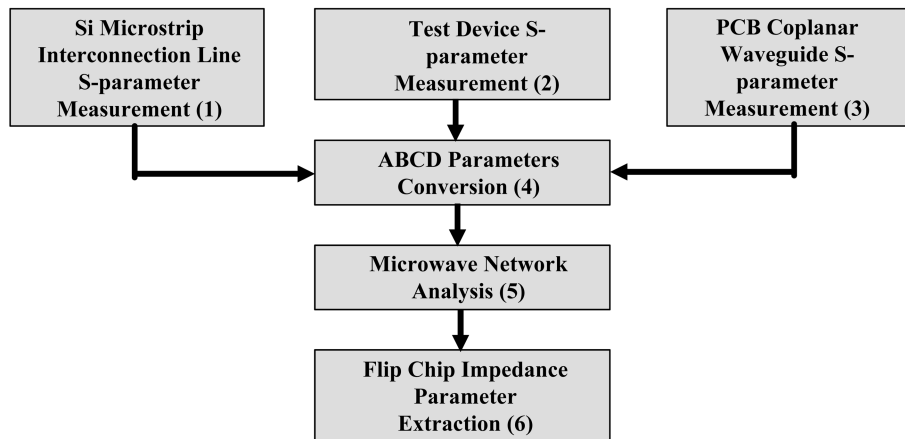


Fig. 4. Extraction procedure for flip-chip interconnection model parameters from the S-parameter measurements and microwave network analysis.

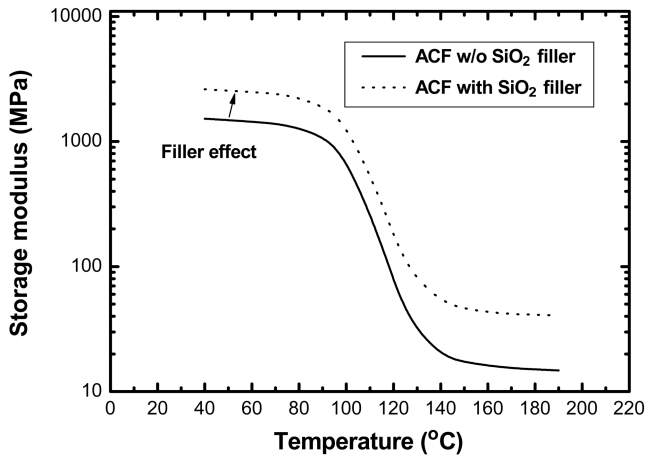


Fig. 6. DMA curves of ACFs samples with different content fillers.

To take the CTE measurements of the ACF samples with different filler contents, TMA (TA Instruments) was used. The TMA curve shows the dimensional change of the cured ACFs as a function of temperature. The CTE value refers to the slope of the TMA curves, and T_g is defined as the deflection point of the TMA curves. Figure 5 shows the CTE measurements of the ACF composite below T_g , defined as α_1 , as well as the CTE measurement above T_g , defined as α_2 . The figure shows that these CTE values decreased when a nonconductive filler was added. This decrease is advantageous because a low CTE value of ACFs is important for improving the reliability of the ACF flip chip assembly.

3.1.2. Modulus measurements of ACFs

Figure 6 shows the variation of the storage (E') of two ACFs with different filler content as a function of temperature. The modulus of the ACF materials, particularly the storage modulus, increases as the silica content increases at room temperature, and the modulus decreases as the temperature increases. For underfill materials of the solder ball flip chip assembly, a high modulus is needed to effectively redistribute the stress of the solder joints to the chip and substrate through the assembly warpage^[11]. Similarly, because the ACF materials assembled on an organic substrate must function as both the underfill and the electrical conductor, high filler content is required to ensure a high ACF modulus.

3.1.3. Dielectric Property Measurement of ACFs

Figure 7 shows the behavior of the dielectric constant of ACFs with different silica filler content as a function of frequency. When the SiO_2 concentration increases from 0 wt% to 40 wt%, which is equivalent to 25.6 vol%, the dielectric constant decreases from 4.2 to 3.5 at 10 MHz, and from 3.4 to 2.8 at 1.8 GHz. On the basis of the composite theory, we expected the dielectric constant of the ACF to decrease^[12]. Adhesives that have a low dielectric constant adhesive are

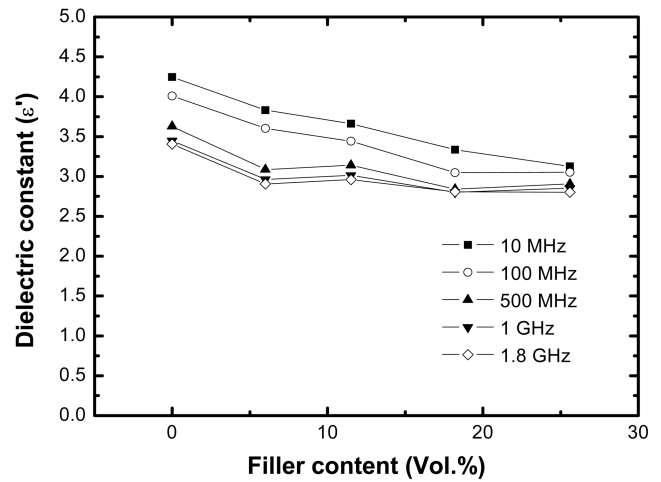


Fig. 7. Dielectric constant behavior of ACF samples with different non-conductive filler content as a function of frequency.

preferred as an interconnect material in high-speed flip chip packages; furthermore, the addition of a nonconductive filler with a low dielectric constant is needed in the ACF formulation for use in a high frequency device package.

3.2. High-Frequency Characteristics of ACF Flip Chip Interconnects

3.2.1. Effect of the dielectric property of ACF on impedance parameters

The effect of a low dielectric filler addition on the high-frequency behavior of ACF was investigated. Figure 8 shows the extracted impedance model parameters of a $100 \mu\text{m} \times 100 \mu\text{m}$ bonding pad for a conventional ACF with a conductive ball only, as well as a low-k ACF with a conductive ball and SiO_2 filler.

In the ACF flip chip interconnect at high-frequency, the interconnection capacitance that forms between the CPW of the PCB and the test chip bump is relatively high due to the high dielectric constant of the ACF resin and the large area; in addition, the gap of the parallel metal plate is smaller than that of the solder ball flip chip structure. Therefore, the resonance frequency of the ACF flip chip interconnect is lower than that of the solder ball flip chip interconnect.

The conventional ACF has a resonance frequency of around 13 GHz, whereas the ACF with the added SiO_2 has a resonance frequency of 15 GHz. This resonance phenomenon was dominantly affected by the inductance of conductive particles and the capacitance of the polymer matrix. In particular, the capacitance of the polymer matrix was induced by the proximity effect of the chip bump and the substrate electrode. Interestingly, the ACF with the SiO_2 has a slightly higher resonance frequency than the conventional ACF. The ACF with the SiO_2 filler exhibited resonance phenomena at around 15 GHz. The difference in resonance frequency originates from a change in the dielectric constant of

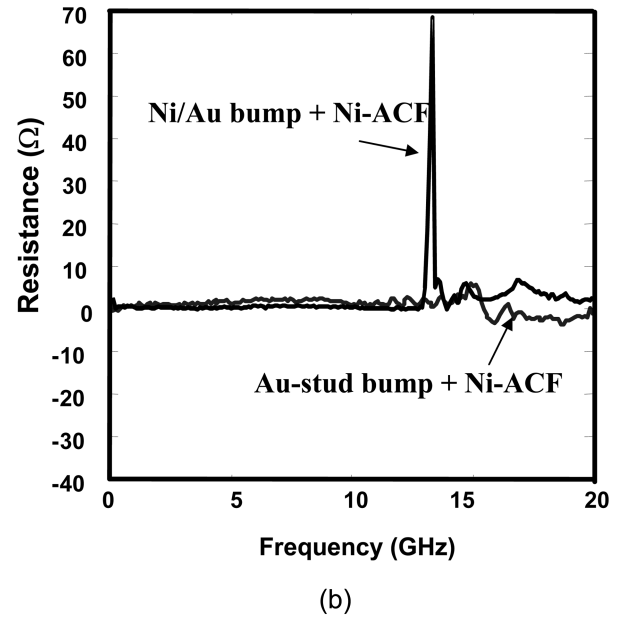
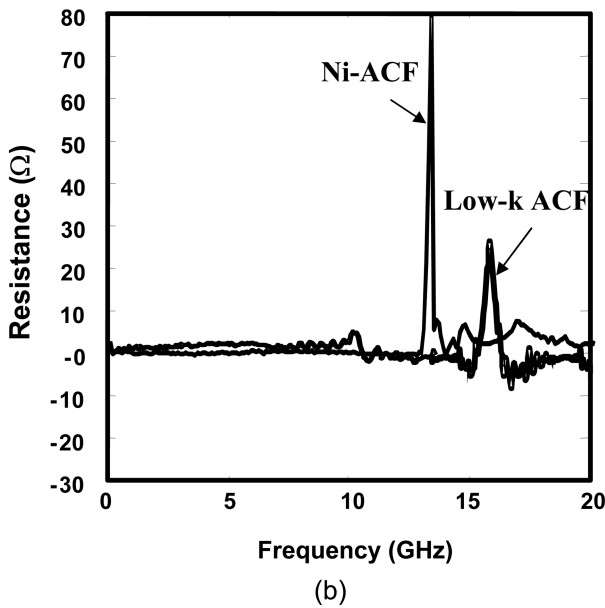
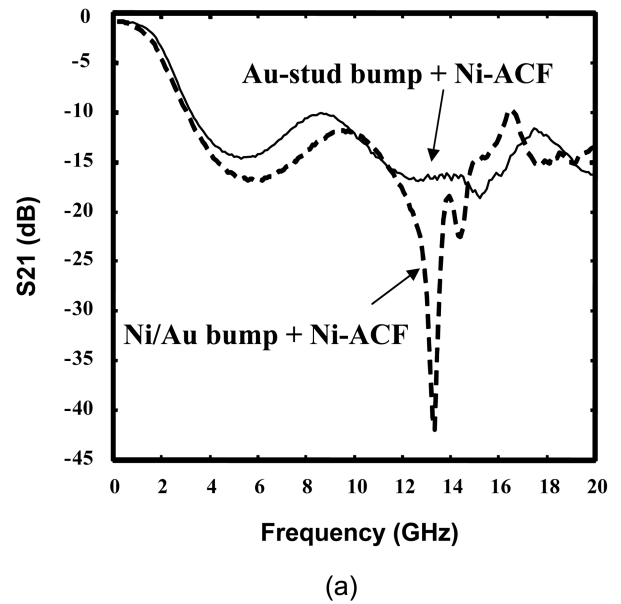
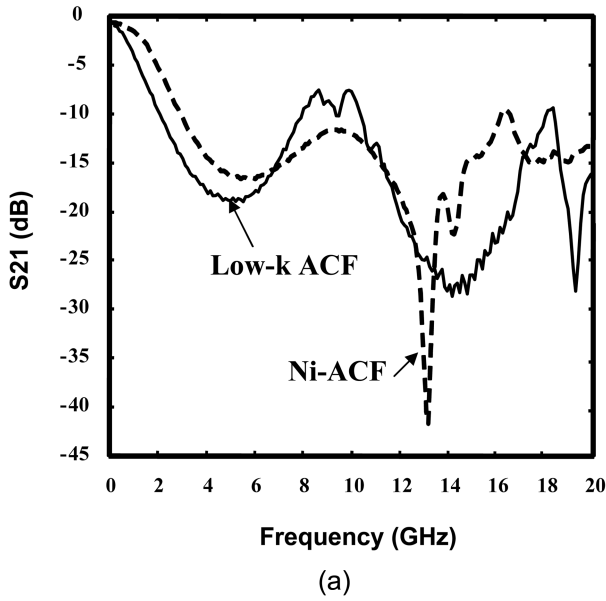


Fig. 8. Impedance parameters, resistance (R) of a flip chip interconnect employing electroless Ni/Au bumped chip and two different ACFs in a high-frequency range.

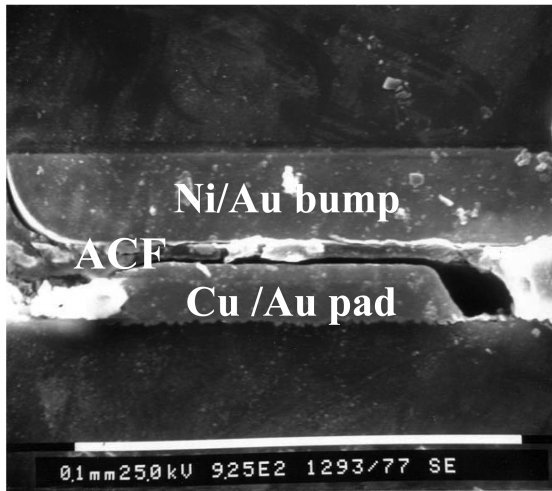
Fig. 9. Impedance parameters, resistance (R) of a flip chip interconnect employing ACF without silica and two different chips, electroless Ni/Au bumped and Au stud bumped chip, in a high frequency range.

the polymer matrix. When the SiO_2 is added to the ACF formulation, the dielectric constant of the polymer matrix in the ACF is lowered in accordance with the ACF's dielectric property and the resultant ACF resonance shifts to a higher frequency.

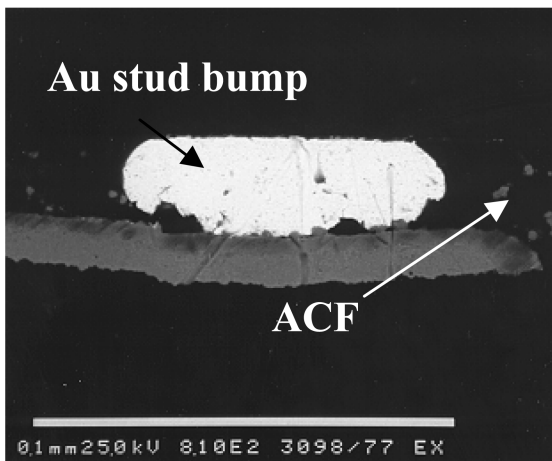
3.2.2. Effect of the bump system on the impedance parameters

The effect of bump metallurgy on the high-frequency behavior of the ACF interconnects was investigated. Figure 9 compares the impedance parameters of the Au stud

bumped chip packaged by the ACF method with those of the Ni/Au bumped chip. As shown in Fig. 9, the Au stud bumped chip shows no resonant phenomena up to 20 GHz. This lack of resonant phenomena means that the Au stud bumps maintain a constant impedance in a high-frequency range up to 20 GHz. In addition, the capacitive coupling of the Au-stud bump interconnect between the chip and the substrate is lower than that of the ACF flip chip with the Ni/Au bumped chip for several reasons: the large gap of epoxy resin, the small area in the parallel pad structure, and the low inductance of the Au stud bump interconnect. Figure 10



(a)



(b)

Fig. 10. Cross-sectional views of ACF flip chip interconnects employing (a) electroless Ni/Au bumps and (b) Au stud bumps.

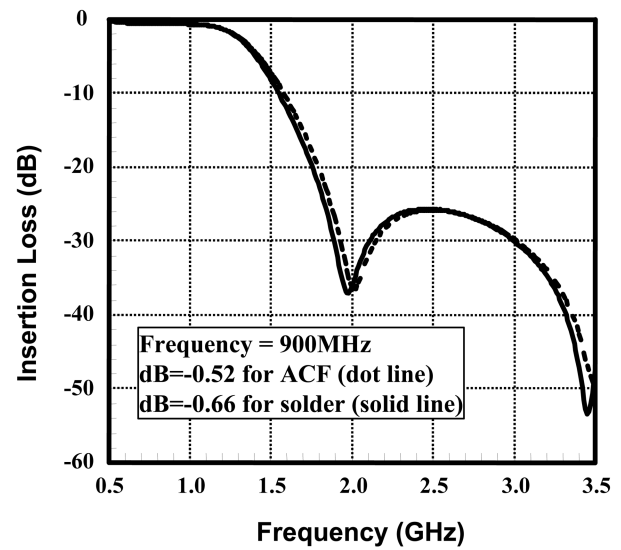
shows the cross-sections of the ACF flip chip interconnects that use the Au stud bumps and the Ni/Au bumps, indicating the structural differences between the interconnects of the two types of bumps.

Consequently, the resonance frequency of the Au stud bump interconnects with the ACF is higher than that of the ACF flip chip interconnect with the electroless Ni/Au bump, and we observed no resonance frequency up to 20 GHz. Thus, to identify the resonance frequency behavior of the ACF flip chip interconnect with Au stud bumps, it is necessary to characterize the impedance parameter over 20 GHz.

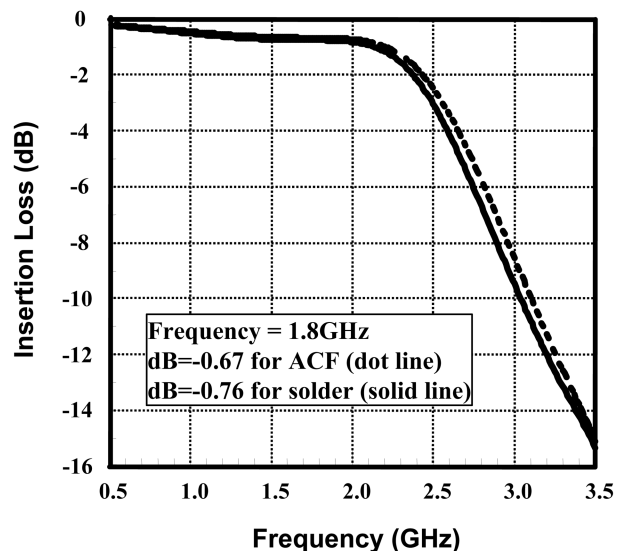
3.3. High-Frequency Characteristics of an ACF Flip Chip with Functional ICs

3.3.1. IC assembly for RF IPDs

A wafer scale CSP package with a solder ball flip chip is widely used in RF IPDs to reduce the form factor. Figure 11



(a)



(b)

Fig. 11. RF performances of low pass filters; (a) 900 MHz filters and (b) 1800 MHz filters packaged using ACF and a solder bump ball.

shows the RF performances of 900 MHz and 1800 MHz lumped low pass filters of flip chips packaged by ACF and solder balls. Fig. 11(a) shows the insertion loss for the 900 MHz low pass filter, 0.52 dB in the ACF flip chip and 0.66 dB in the solder ball flip chip. This shows that the high-frequency performance of the RF IPDs is similar for both package methods, and that there is no degradation in the high-frequency characteristics of the RF IPD packaged by ACF. In Figure 11(b), similar performance in the high-frequency range for the 1800 MHz low pass filter can be observed.

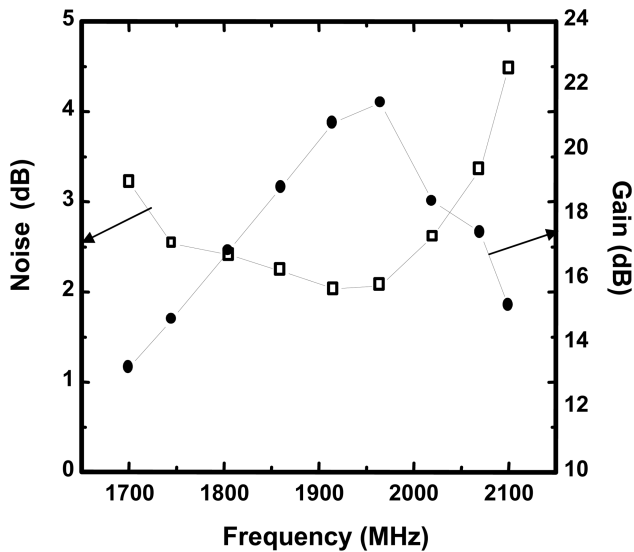


Fig. 12. RF performance of MMICs packaged by ACF flip chip method; noise and gain of the LNA function for a PCS downconverter.

3.3.2. IC Assembly for RF MMIC

Figure 12 shows the RF performances of the MMICs packaged by the ACF flip chip method with respect to the gain and noise of the LNA function for a PCS downconverter. The solid circle and line correspond to the measured gains, and the solid square and line correspond to the measured noise. The measured noise is less than 2.5 dB for the range of 1.8 GHz to 2.0 GHz. The measured gain is greater than 16 dB within the same frequency range. This LNA chip was originally designed to exhibit 1.5 dB of noise and 15 dB of gain for a range of 1.8 GHz to 2.0 GHz. In addition, it has the form of an MLF plastic package in which the wire bonding on the lead frame is used for the electrical interconnection, and the plastic molding is used for protection. Although the LNA module for the PCS application of the ACF flip chip was not finally tuned for the design performance, these results indicate that when a simple ACF flip chip method is employed, no functional degradation occurred in the replaced interconnection. Hence, the high-frequency performance of the ACF flip chip interconnect in a functional RF MMIC module has been successfully demonstrated.

4. CONCLUSION

We investigated the high-frequency performances of several flip chip interconnects with anisotropic conductive

adhesives, at the RF and high-frequency range. For high-frequency flip chip applications, ACF materials with a low dielectric constant, low CTE, and a high modulus were developed. To investigate the high-frequency characteristics of the ACF flip chip interconnects, the high-frequency model parameters were measured, and our analysis was based on an ACF flip chip model and network analysis with test vehicles made of different bonding materials and bump metallurgies. For real application of an ACF interconnection at the RF and high-frequency range, a passive device comprised of an RF IPD and an active device comprised of a highly integrated MMIC was used on an RF module. Both devices showed good RF performances. In conclusion, flip chip technology that uses ACF is simple and cost effective for high-frequency devices.

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