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Materials Science and Microelectronics

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We demonstrate using examples that materials science played a crucial role in the evolution of microelectronics in the past, its significant current role and its envisaged role in the future as device dimensions decrease substantially. The technical challenges are significant because we do not fully understand the behavior of materials at extremely small length scales.

Keywords: electromigration, Schotty and Ohmic contacts, dislocations in III-V crystals, microstructures of mixed III-V layers, integration of dissimilar materials, low-dimensional structures

1. INTRODUCTION

The evolution of microelectronics constitutes one of the most important developments of the 20th century. It has permeated every aspect of our life. We depend on it for communication, data storage, transportation, medical care, etc. We depend on it when we get up in the morning until we go to bed. It is hard to conceive a lifestyle without it.

Since the demonstration of the transistor effect at Bell Telephone Laboratories in the late 40s, three disciplines contributed substantially to the development of microelectronics: solid state physics, electrical engineering, and materials science. The solid state physicists developed concepts for novel devices. The electrical engineers designed circuits incorporating these novel devices, resistors, capacitors and inductors that could perform various functions. The materials scientists provided a bridge between the two disciplines and made their ideas a reality. For example, the concept of semiconduction was known by the early thirties. However, it could not be demonstrated in Ge until Bill Pfann of Bell Laboratories was able to purify it to very high levels using the concept of zone refining. We can cite many such examples where materials science played a crucial role in making microelectronics a reality. It is the author's considered opinion that like any other age in the development of human civilization that is linked to a material type, we should refer to the present age as the "Materials Age."

The principal objective of this paper is to sensitize the reader as to the role of materials science in microelectronics in the past, the present and the future. Since this topic is very vast and can only be covered cursorily, the choice of examples will be colored by the author's preferences. However, we will demonstrate that materials science played a crucial role in the emergence of microelectronics in the past, is playing a significant role in the present, and will do so in the future.

2. PAST ROLE

We have chosen the following two topics to illustrate the role of materials science in microelectronics in the past: electromigration in interconnects and transformation of Schottky contacts into ohmic contacts on annealing.

Metallizations serve two functions in the semiconductor technology. Metallizations that provide connections between different devices and components on a chip are termed interconnects. Metallizations that allow an electrical signal to enter in and come out of a semiconductor are referred to as contacts. Both types of metallizations form the backbone of microelectronics.

2.1. Electromigration in Interconnects

In metal-oxide-semiconductor-field-effect-transitions (MOSFETs) interconnection delays depend on the so-called RC time constant, where R and C are, respectively, the effective total resistance and capacitance of the device at the gate and interconnection level. The higher the value of RC, the lower the speed of the device. We can write RC[1]

$$RC = \frac{S}{t}\frac{L^2\varepsilon_{ox}^2}{t_{ox}} \quad (1)$$

where S, L and t are, respectively, length and thickness of the interconnect and E_{ox} and t_{ox} are permittivity and thickness of the oxide that separates the interconnect from the semiconductor. With decreasing device dimensions and increasing circuit complexities, the length L of the interconnects is becoming larger. To keep RC low, we would like to reduce

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L. We can effectively reduce L if interconnections are carried out in more than one plane, separated from each other by insulating layers. We refer to the approach as a multilevel interconnection scheme[2]. The schematic in Fig. 1 illustrates this concept.

Interconnects are very thin, narrow metal lines that carry high, direct current densities. As a result, mass transport occurs in thin film conductors, which is referred to as electromigration. In silicon technology, involving Al interconnects, electromigration is manifested as hillocks on film surfaces as shown in Fig. 2(a), as bridges between two conductor lines as depicted in Fig. 2(b) and a discontinuity in a conductor line as shown in Fig. 2(c)[3].

The integrated circuits (ICs) made their commercial appearance in 1966. In the early seventies, IBM experienced a serious problem with their ICs that was attributed to electromigration-induced failures of the type shown in Fig. 2. This problem was apparently resolved by the addition of a small amount of Cu to Al[4]. We still do not understand what role Cu has in enhancing the electromigration resistance of the Al interconnects.

The mechanism governing electromigration is not well understood. At high current densities, electrons can exert sufficient force on atoms to remove them from their lattice sites and propel them, resulting in a net flux of atoms toward the anode. This force is referred to as "electron wind." In polycrystalline interconnects, divergences occur in atomic fluxes at grain boundary triple points, leading to either local accumulation or local depletion of mass. These local mass changes lead to the formation of hillocks, Fig. 2(a) and voids, Fig. 2(c). If hillocks grow sufficiently, they can flip onto their side and short the contiguous conductor lines, Fig. 2(b). On the other hand, the continued growth of voids could lead to discontinuities in a conductor. The activation energies associated with electromigration have also been measured in a number of interconnects. These measurements indicate that the electrotransport in films occurs by the movement of atoms along grain boundaries, i.e., by grain boundary diffusion.

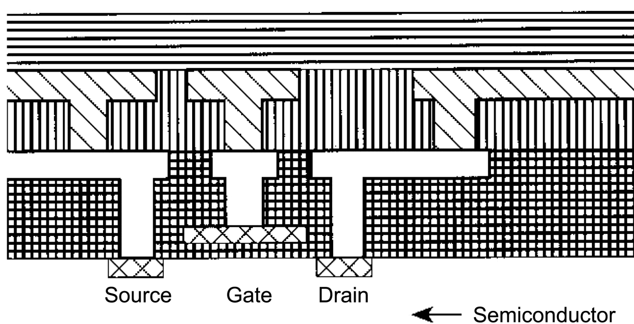
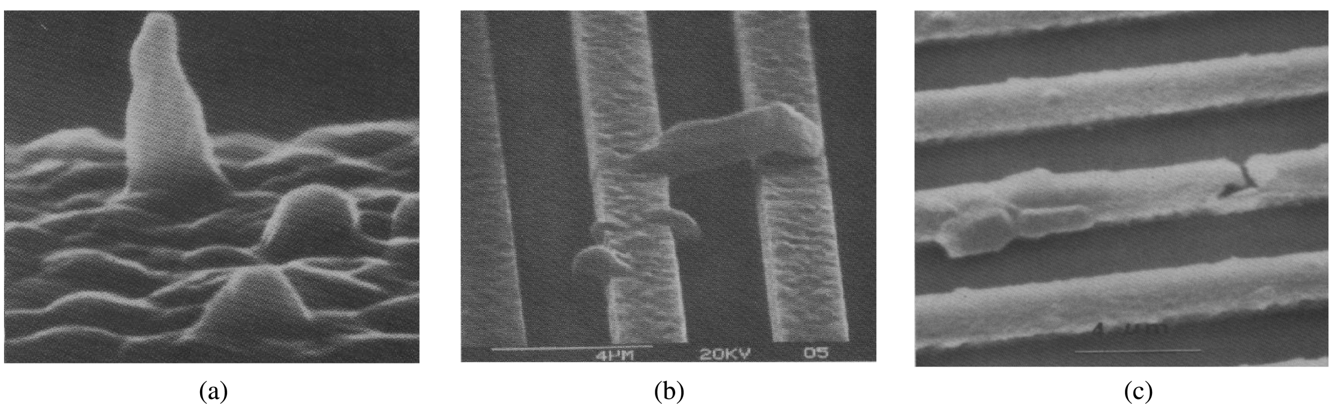


Fig. 1. Schematic showing multilevel interconnects in a MOSFET. The cross-hatched regions represent the source, drain and gate contacts. Heavy-bordered regions represent different levels of metal interconnects isolated by the insulator films[1].

The prevention of electromigration-induced damage in interconnects is a formidable challenge for materials scientists. Since the occurrence flux divergences at grain-boundary triple points produces damage, reducing the number of triple points per unit area, i.e., increasing the grain size, should enhance electromigration resistance. Of course, single-crystal films would make ideal interconnects because the flux-divergence sites would be eliminated, but it is not feasible to deposit such films on amorphous SiO_2 films.

The introduction of <111> texture in Al film increases their electromigration resistance[3]. This observation is not well understood. However, it demonstrates that the nature of grain boundaries has a profound effect on electromigration resistance of an interconnect. We need to understand the role of grain boundaries in electromigration and then engineer them to enhance damage resistance of interconnects.

In state-of-the-art silicon technology, Al based interconnects are being replaced by copper. This is principally for one reason. The melting point of Cu is substantially higher than that of Al. This implies its cohesive energy is higher,



(a) (b) (c)

Fig. 2. (a) Manifestations of electromigration damage in aluminum films: hillock formation[3].
(b) Manifestations of electromigration damage in aluminum films: whisker bridging between two conductor lines[3].
(c) Manifestations of electromigration damage in aluminum films: mass accumulation and depletion[3].

leading to a higher value for activation energy for grain boundary diffusion in Cu.

2.2. Schottky to Ohmic Transition in Contacts

When a metal is deposited on a semiconductor, the composite structure exhibits current (I)-voltage (V) characteristics which resemble that of a p-n junction. The composite is referred to as a Schottky contact. However, by annealing the I-V characteristics this can be changed to linear I-V behavior, and this behavior is called ohmic. An interesting question is what changes do occur at the metal-semiconductor interface that lead to the ohmic behavior because the electronic behavior of the junction is dictated by this interface?

To illustrate the role of materials science in understanding the Schottky to ohmic transition, we have chosen Au/Ge/Ni/Au contacts to n-GaAs [5]. Attempts were made to correlate the electrical properties of these contacts to the atomic structure, chemistry, phase distribution and morphology at the metal-semiconductor interfaces. It was observed that in the as-deposited state, the multi-layer metallization consisting of Ni/Au/Ge/Au forms a Schottky barrier with the underlying (001) n-GaAs [6]. When the metal-semiconductors were annealed at progressively higher temperatures in the range 350°C to 500 °C, the I-V characteristics of the contacts changed from Schottky to ohmic [6]. This is illustrated in Fig.

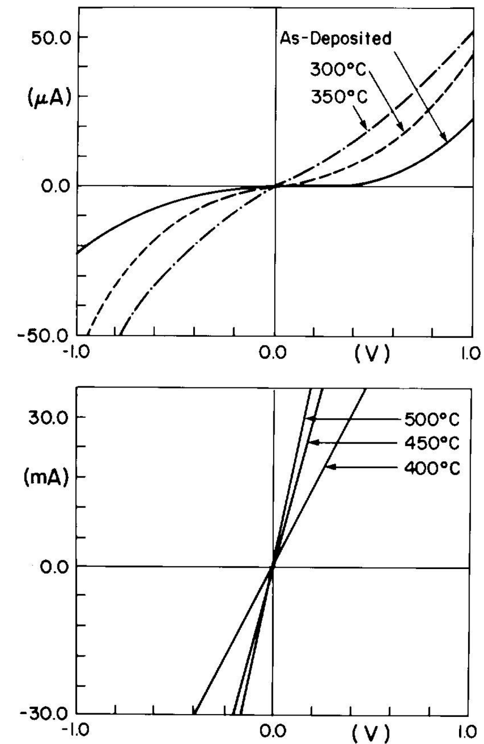


Fig. 3. I-V characteristics of as-deposited and annealed Ni/Au/Ge/Au contact to GaAs.

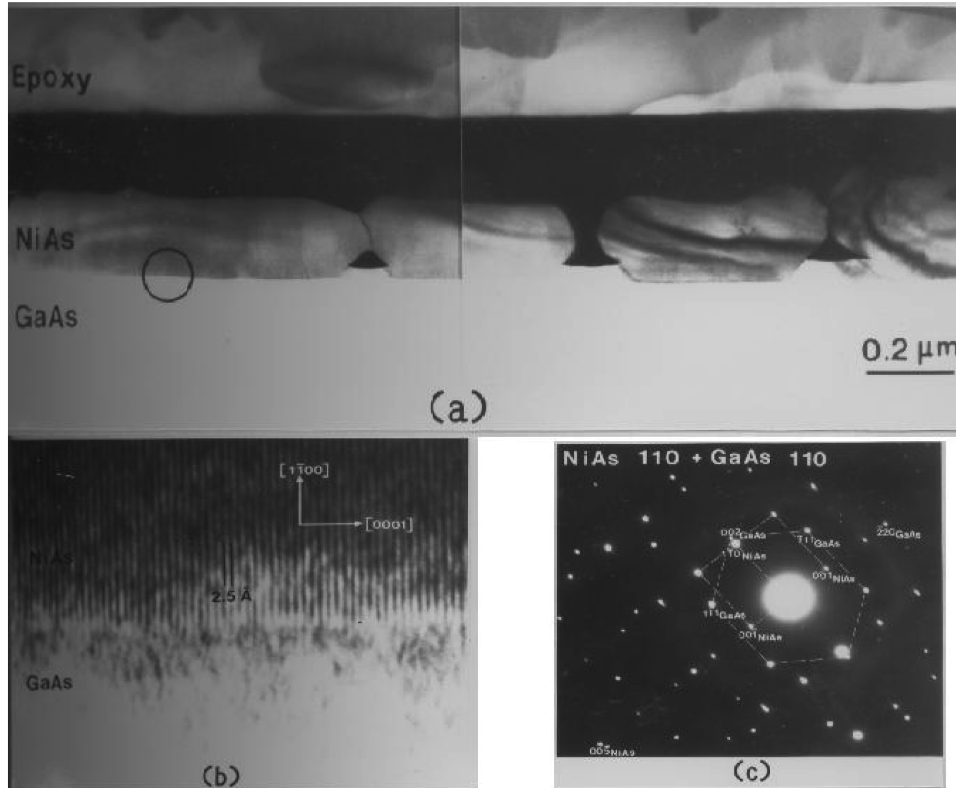


Fig. 4. (a) Cross-sectional bright-field image of the Ni/Au/Ge/Au contact to GaAs after annealing at 500 °C for 10 min, showing big NiAs particles at the interface. (b) Lattice image obtained from the circled area in (a). (c) Corresponding diffraction pattern showing the orientation relationship between NiAs and GaAs.

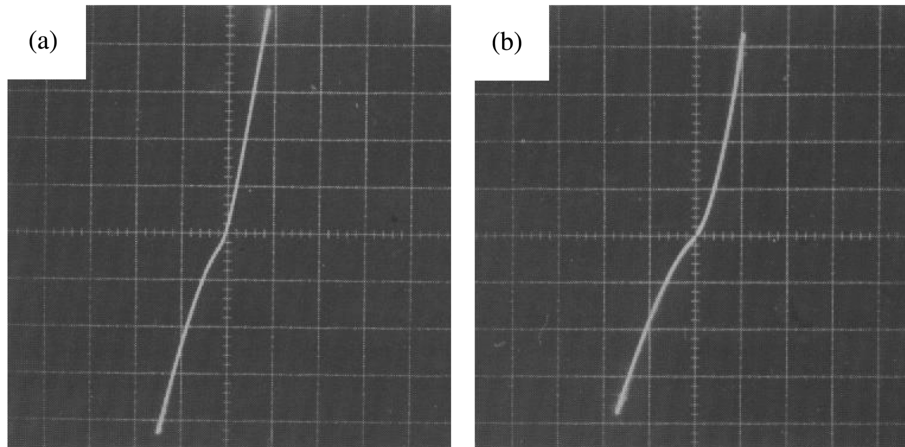


Fig. 5. I-V characteristics of as-grown multi-layer structures: (a) 50 nmNiAs/30 nm Ge/250 nm GaAs:Si ($\sim 1 \times 10^{17}$cm^{-3})/1 μm n^+ - GaAs:Si (2×10^{18}cm^{-3}) – structure B and (b) 30 nm Ge/50 nm NiAs/250 nm-GaAs:Si ($\sim 1 \times 10^{17}$cm^{-3})/1 μm n^+ - GaAs:Si (2×10^{18}cm^{-3}) – structure C. The I-V characteristics of structure A (not shown) were rectifying with a Schottky barrier height of .73 V.

3 taken from the study of Kim[6]. The lowest contact resistance was observed after annealing at 500 °C. The concomitant study of the metal-semiconductor interface by transmission electron microscopy revealed that the majority of the interface is covered with NiAs grains that are epitaxial with the underlying substrate as shown in Fig. 4 [6].

An interesting question is what role does Ge have in producing low resistance contacts? To address this issue, Rai *et al.*[14] grew the following multi-layer structures by molecular beam epitaxy: NiAs/n-GaAs, NiAs/Ge/n-GaAs and Ge/NiAs/n-GaAs. They evaluated the electrical characteristics of the layered structures and also investigated various interfaces using high resolution electron microscopy (HRTEM). They showed that NiAs forms a Schottky barrier with n-GaAs and the barrier height is 0.73 eV. On the other hand, the other two structures were found to be weakly rectifying at room temperature as shown in Fig. 5[7], and thus their barrier heights could not be measured.

Figure 6 shows the HRTEM images of various interfaces in the three structures[7]. The NiAs/GaAs interface in Fig. 6(a) is slightly rough, shows steps and contains misfit dislocations. Figure 6(b) shows the Ge/GaAs and NiAs/Ge interfaces in the NiAs/Ge/GaAs structure. The former is barely discernable, whereas the latter is quite rough on the atomic scale. Also, NiAs is highly devective. Figure 6(c) shows HRTEM images of the NiAs/GaAs and Ge/NiAs in the Ge/NiAs/GaAs structure. A transition region, ~1.5 nm thick, is observed between the NiAs layer and GaAs that is not visible in Fig. 6(a).

Rai *et al.*[14] argued that the as-deposited NiAs/Ge/GaAs structure is weakly rectifying because the GaAs contiguous to Ge could be highly doped, leading to a tunneling contact. However, in the case of the Ge/NiAs/GaAs structure, they suggested that Ge could diffuse through the open structure of NiAs and accumulate at the NiAs/GaAs interface, again

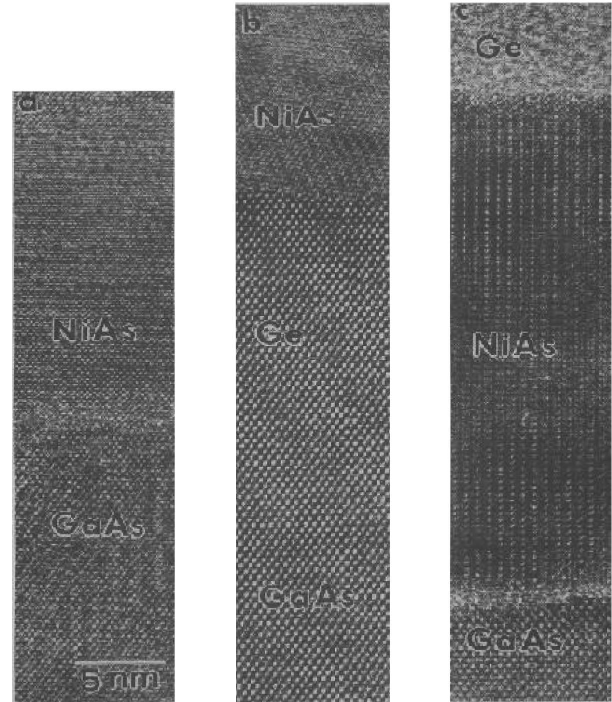


Fig. 6. Cross-sectional high resolution transmission electron micrograph showing different interfaces in various structures: (a) The NiAs/GaAs interface in structure A; orientation for GaAs is [110], whereas it is [01$\bar{1}$1] for NiAs. (b) The Ge/GaAs and the NiAs/Ge interfaces; orientation of Ge and GaAs is [110], whereas it is [11$\bar{2}$0] for NiAs. (c) The Ge/NiAs and the NiAs/GaAs interfaces in structure C; orientation of GaAs is [110], whereas it is [11$\bar{2}$0] for NiAs. The Ge layer consists of amorphous and highly defective crystalline regions.

resulting in heavy doping of GaAs. So, it is Ge that has the major role in producing ohmicity and NiAs is only a facilitator.

3. PRESENT ROLE

We have chosen the following two topics to illustrate the present role of materials science in microelectronics: reduction of dislocations in III-V crystals and microstructure of active layers of emitters for lightwave communication systems. It will be apparent from the following that we need substrates with low dislocation densities to fabricate reliable emitters.

3.1. Reduction of Dislocations in III-V Crystals

There is a consensus that in devices, such as solar cells, light emitters, bipolar transistors, photo detectors, etc., whose action is governed by the migration of minority carriers, the influence of dislocations on yield, performance and reliability of devices is very dramatic [8]. On the other hand, the effects of dislocations on the performance of majority carrier devices, such as MOSFETs, are not that dramatic.

We require multi-layer structures for devices, such as light emitters and detectors based on III-V materials. We use substrates obtained from bulk crystals as platforms for the deposition of these structures. Since there is one to one replication of dislocations present in the substrate into multi-layers [9], we need bulk crystals with low dislocation densities.

To familiarize the reader with the growth of III-V crystals, we show in Fig. 7 a setup that is used for the growth of InP crystals. The process is referred to as the liquid-encapsulated Czochralski technique (LEC), a modified version of the Czochralski process used for the growth of Si crystals. Since the vapor pressure of group V species over the III-V melts is extremely high, the growth is carried out in a pressure vessel. In addition, a thin layer of boric oxide covers the melt to prevent the escape of group V species. There is a source of P in the vessel to maintain stoiciometry.

Dislocations in crystals could originate from three different sources: (1) dislocations present in the seed crystal could propagate into a growing crystal, (2) excess point defects inherited during cool down from the melt could cluster to form dislocation loops, and (3) under the influence of thermal-gradient-induced stresses which prevail during growth, dislocations could multiply. We can eliminate the first source using high quality seeds.

The second source of dislocations is the excess concentration of point defects that is incorporated into a crystal that is grown from a high temperature. Clustering of point defects into faulted dislocation loops during the cool down can eliminate supersaturation. The driving force for the formation of these loops is the overall reduction in the energy of the system. As an example, let us evaluate the energy change ΔE associated with clustering of n interstitials into a dislocation loop of radius R. We can show that ΔE is given by

$$\Delta E = 4\pi n r^2 \gamma - 2\pi R^2 E_{SFE} - \pi R G b^2 \quad (2)$$

where r is the radius of an interstitial, γ is the surface energy of an interstitial, E_{SFE} is the stacking fault energy of the crystal, G is the shear modulus, and b is the Burgers vector of the dislocation that bounds the loop. Since a large number of interstitials are involved on the formation of a loop, the term n γ in Equation (2) is fairly large. Therefore, substantial savings in the internal energy of the crystal can occur if interstitials cluster together to form loops. When the term $4\pi n r^2 \gamma$ is greater than $2\pi R^2 E_{SFE} + \pi R G b^2$, point defects will cluster together to form loops.

Since crystals are grown under conditions which are far from equilibrium, we will always have supersaturation of point defects in growing crystals. An interesting question is can we do anything to prevent them from clustering? One

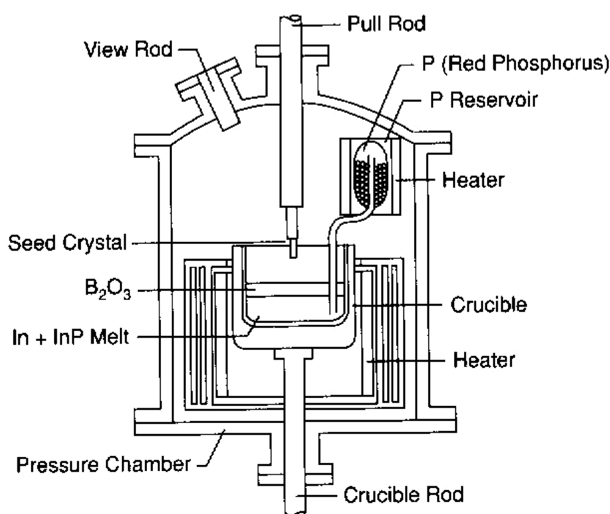


Fig. 7. Schematic of an LEC setup for the growth of InP crystals[10].

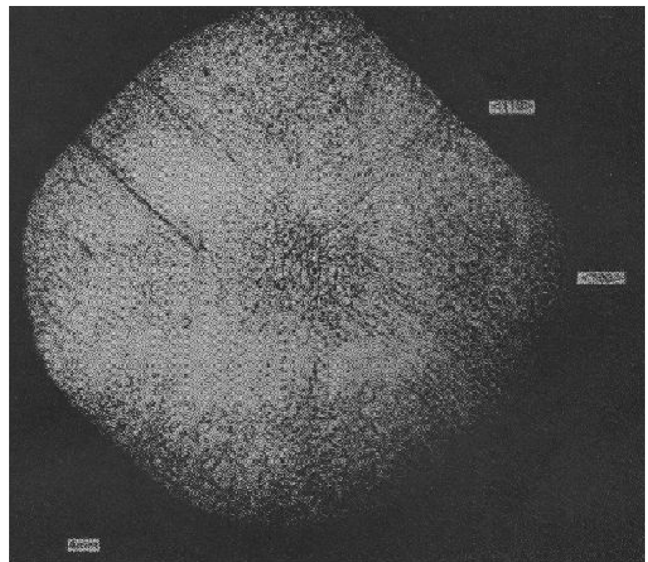


Fig. 8. Macrophotograph obtained from a KOH-etched (001) GaAs wafer. The wafer was cut from the top end of a tellurium-doped GaAs boule grown by the LEC technique[11].

approach could be to bind vacancies and interstitials by the addition of suitable isoelectronic impurities. Considering the fact that there are two types of vacancies and two types of interstitials and defects are charged in III-V compound semiconductors, the addition of impurities to bind point defects may not be practical.

The thermal-gradient-induced stresses constitute the major source of dislocations in III-V crystals grown by the LEC technique. Etch pit patterns observed on substrates, Fig. 8, and their excellent match with those computed by thermoelastic calculations, Fig. 9, support the preceding assessment [8,11]. Therefore, to reduce dislocations in crystals we need to develop an approach that negates the effects of thermal-gradient-induced stresses. A generic approach was developed that entailed the addition of isoelectronic impurities and dopants whose covalent tetrahedral radii differ from those of the host lattice atoms. The addition of suitable impurities raised the yield strength of crystals, thereby reducing the probability of dislocation multiplication [12-16].

When an impurity is added to a tetrahedrally coordinated crystal, the bond lengths in the tetrahedron either increase of decrease, depending on the covalent tetrahedral radius of an impurity; covalent tetrahedral radii of various atoms are listed in Table 1. It was observed that the addition of 1 at % In reduces substantially the density of dislocations in GaAs crystals. The substitution of Ga by In on the Ga-sub lattice changes bond lengths in GaAs. The Ga to As bond length is 0.244 nm (0.126 nm + 0.118 nm), whereas the In to As bond length is 0.262 nm (0.144 nm + 0.118 nm).

The GaAs lattice contains two types of tetrahedra: As- and Ga- centered. Let us first consider the case of an As- centered tetrahedron in which an As atom is tetrahedrally coordinated to four Ga atoms. Four distinct tetrahedral units may form when we replace some of the Ga atoms with In atoms: As(Ga3In), As(Ga2In2), As(GaIn3) and As(In4). The bond lengths within the tetrahedra are different, resulting in different volumes and distortions. The substitution of Ga on the Ga-centered tetrahedron by In leads to volume increase, but there are no distortions because the four In-As bonds are equal in length.

Ehrenreich and Hirth[37] modeled the interaction of dislocations with the above strain centers. They showed that the presence of these strain centers would lead to solid solution strengthening of the GaAs lattice. As a result, dislocation density is reduced because dislocation glide is made more difficult. Their argument works well for isoelectronic impurities where we need to consider only the size interaction. However, with dopant impurities, the situation is more complicated for two reasons. First, the dopant atoms are ionized. Second, point defects in semiconductors are charged. So, besides the size difference, we need to invoke point defect-dopant interactions to understand the effects of dopants on mechanical properties [17].

Table 1. Tetrahedral covalent radii of different atoms in nm*

	Be	B	C	N	O	F
	0.106	0.088	0.077	0.07	0.066	0.064
	Mg	Al	Si	P	S	Cl
	0.14	0.126	0.117	0.11	0.104	0.099
Cu	Zn	Ga	Ge	As	Se	Br
0.135	0.131	0.126	0.122	0.118	0.114	0.111
Ag	Cd	In	Sn	Sb	Te	I
0.152	0.148	0.144	0.14	0.136	0.132	0.128
	Hg					
	0.148					

*According to Pauling (1960).

3.2. Microstructure of Active Layers of Emitters for Lightwave Communication Systems

Lightwave communication constitutes one of the major technological developments of the 20th century. In this technology, data is transmitted over fused silica fibers as pulses of light. These fibers exhibit minimum dispersion and low losses at 1.33 and 1.55 μm. Therefore, devices emitting at these wavelengths are optimal for the lightwave communication systems. As illustrated in Fig. 10, we can fabricate such emitters based on the InGaAsP/InP system. The elegance of this system is that we can vary the emission wavelength from 1.1 to 1.67 μm, and active layers in an emitter are still lattice-matched to InP.

A typical InGaAs/InP dielectrically isolated, front light emitting diode is shown in Fig. 11. The active layer is InGaAsP that emits at 1.33 μm. Holes and electrons are

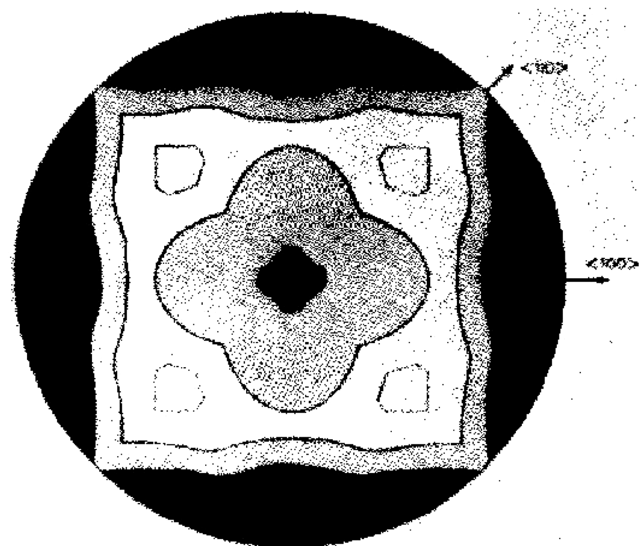


Fig. 9. Dislocation-density contour lines for the top wafer of a (001) GaAs boule computed by Jordan *et al.* (1980).

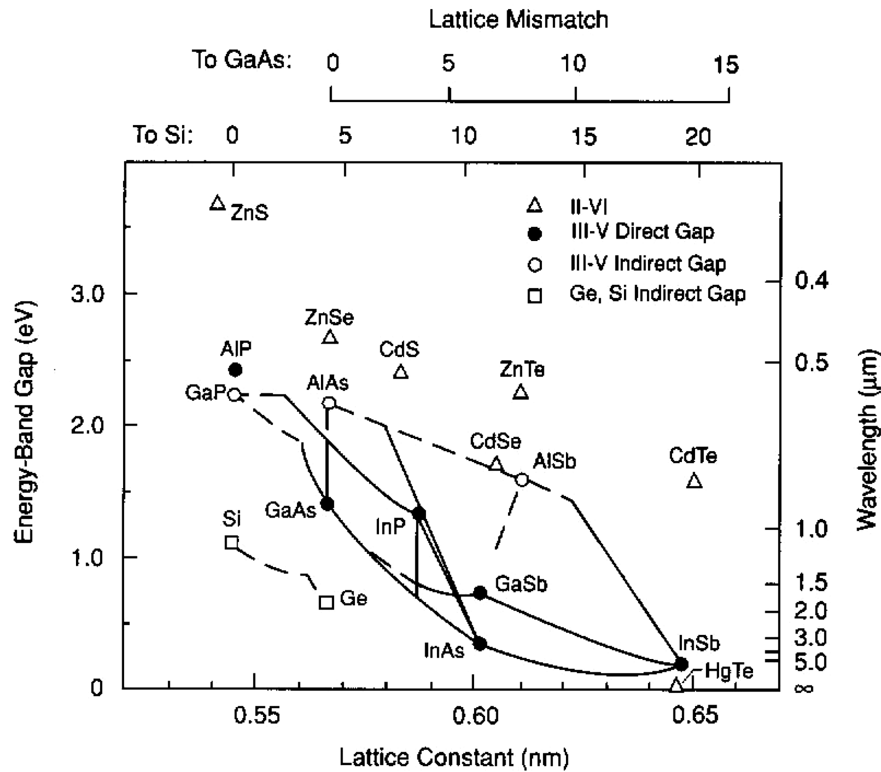


Fig. 10. Band gaps versus lattice constants for III-V, II-VI, and IV semiconductors. The lines joining the III-V compounds give the band gap and lattice constant of ternary layers. Open and closed symbols denote indirect- and direct-gap materials.

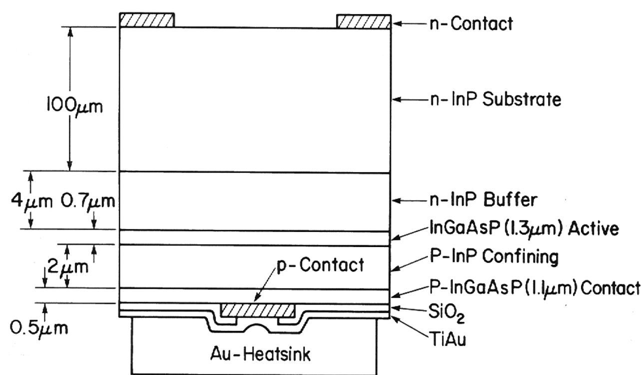


Fig. 11. Schematic of a dielectrically isolated, front-emitting InP/InGaAsP LED[8].

injected into the active layer from the p- and n- side, respectively, by biasing. They recombine in the active layer to generate light. The p- and n- InP layers help in confining carriers to the active layer. Mahajan *et al.*[18], Temkin *et al.*[19] and Mahajan *et al.*[20] used optical pumping to simulate the degradation behavior of InGaAsP/InP based emitters. They showed that slow degradation occurs by the multiplication of dislocations involving non-radiative recombination enhanced glide and climb[18]. On the other hand, the catastrophic degradation occurring at higher pumping levels involves the migration of liquid droplets. This migration produces highly damaged regions[19,20]. They also demonstrated that InGaAsP layers are considerably more degradation resistant that GaAlAs.

To understand the superior degradation resistance, Mahajan and co-workers examined microstructures of $In_{1-X}Ga_XAs_YP_{1-Y}$ layers for various values of x and y. Their results were reviewed by Zunger and Mahajan[22]. The highlights of the results are as follows. The atomic species in $In_{1-X}Ga_XAs_YP_{1-Y}$ are not distributed at random on their respective sublattices. Two types of deviations from randomness are observed: phase separation and atomic ordering. Phase separation is two-dimensional in nature, occurs on the surface while the layer is growing, takes place along soft directions lying in the growth plane and is observed in layers which contain atomic species having differing covalent tetrahedral radii[21,22]. Furthermore, the occurrence of phase separation is independent of the growth technique.

In a mixed layer XYZ_2, the two band lengths, i.e., X-Z and Y-Z, are unequal. Therefore, as argued earlier, the stacking of tetrahedra to build a layer must involve bond stretching and bending, a high strain situation. This energy can be lowered if the layer undergoes phase separation at the surface because most of the bonds within phase separated regions have the same length.

The CuPt-type ordering was observed only in those layers which were grown by vapor phase techniques, but not by liq-

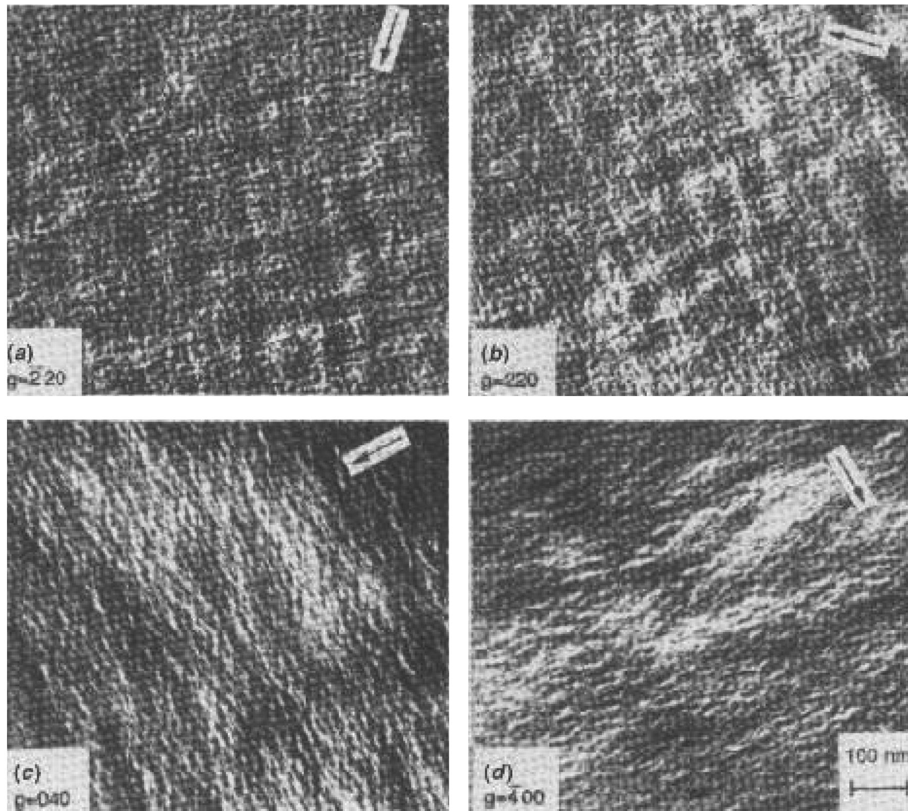


Fig. 12. Electron micrographs (a) – (d) showing the contrast behavior of a phase-separated microstructure observed in a (001) InGaAsP epitaxial layer grown by LPE under different reflections [21].

uid phase epitaxy (LPE), and contain atomic species differing in their tetrahedral radii [23]. Two variants of the ordered structure, instead of four, were observed, implying that atomic ordering occurs on the surface. Phillips *et al.* argued that ordering is caused by (2x4) surface reconstruction induced sub-surface stresses that bias the occupation of sites by atoms differing in their tetrahedral radii[23]. Since reconstruction cannot occur when a surface is covered with a conducting liquid, as in the case of LPE, the absence of ordering in the LPE grown layers can be rationalized.

Figure 12, reproduced from the study of McDevitt *et al.*[21], show microstructure of an InGaAsP layer grown on a (001) InP substrate by LPE under different operating reflections. They observed well-developed satellite reflections in electron diffraction patterns. We can deduce from Fig. 12 that the fine scale speckle structure is due to phase separation along the [100] and [010] directions lying in the (001) growth plane. The observed wavelength of modulations is ~ 8 nm. On the other hand, the coarse dark bands are due to buckling of the surface caused by two-dimensional strains associated with the fine speckle structure [22].

We show in Fig. 13 a (110) cross sectional electron micrograph obtained from a (001) InP/InGaAsP/InP heterostructure grown by vapor phase epitaxy[24]. The speckle structure characteristic of phase separation is seen, Fig. 13(a). In addition, we see two sets of extra spots halfway between the <111> spots in the diffraction pattern, Fig. 13(b). The extra spots are due to CuPt-type atomic ordering. The extra spots were absent in the $[1\bar{1}0]$ pattern, implying that ordering occurs only on two of the possible {111} planes and takes place very close to the surface.

We envisage that the presence of phase separation and atomic ordering in InGaAsP layers enhances the degradation resistance of light emitting devices used in lightwave communication systems. Mahajan[8] suggested that the multiplication of dislocations by nonradiative, recombination – enhanced glide and climb is difficult in phase separated and atomically ordered InGaAsP layers. Since the phase separated regions may have different shear moduli, dislocations may tend to lie in the regions having lower modulus because the energy of a dislocation is proportional to the shear modulus. During glide, the dislocations must traverse the high shear modulus regions, which requires additional energy and makes glide difficult. Likewise, the motion of dislocations through ordered regions produces antiphase boundaries that are a high energy situation. The climb of dislocations in ordered structures is also difficult because its occurrence creates antiphase domain boundaries. In addition, the activation

energy for climb is increased in the presence of atomic ordering[25]. Since dislocation glide and climb in phase separated and ordered layer is difficult, we can rationalize the observed enhanced degradation resistance of InGaAsP layers.

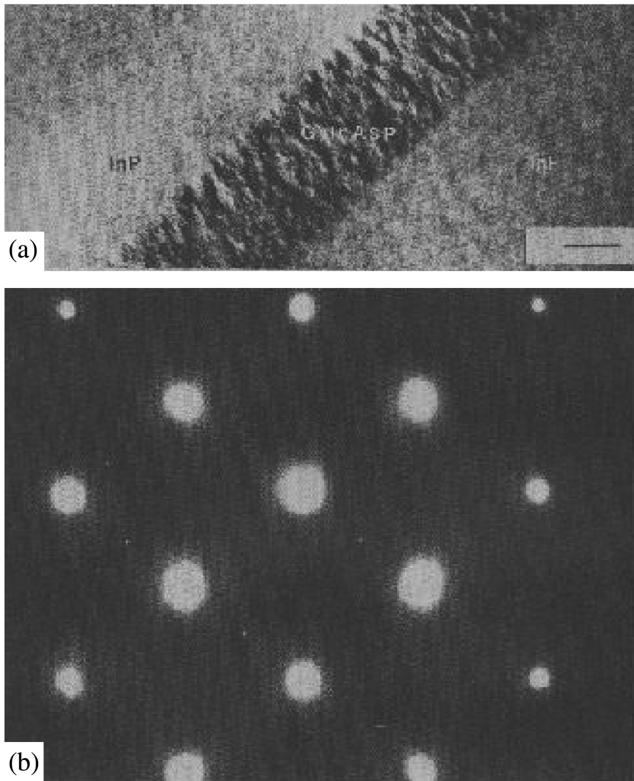


Fig. 13. (a) Electron micrograph showing the (110) section of a heterostructure grown by the vapor levitation technique and (b) the diffraction pattern[24].

4. FUTURE ROLE

To illustrate the role of materials science in microelectronics in the future, we have chosen two challenging problems: integration of dissimilar materials and growth of low-dimensional structures. The success in integration could lead to systems-on-a-chip, whereas the growth of nanowires and quantum dots could result in fast and novel devices. In the following, we highlight challenges facing both of these problems and discuss some plausible solutions.

4.1. Integration of Dissimilar Materials

Since lattice parameters of materials being integrated are usually different, there are two types of contributions to the energy of a heterointerface: strain and electronic. If we were to intergrate them using epitaxy, the initial growth may occur via either the Stranski-Krastanov mode or the Volmer-Weber mode. When the energy of the heterointerface is low, a continuous film is produced when growth islands constituting either of the two modes spread laterally and coalesce. On the other hand, if interface energy is large, we may never obtain a continuous film. Instead, islands may grow vertically into isolated pillars, a very undesirable situation.

Akasaki *et al.*[36] proposed a very ingenious solution for the growth of GaN on (0001) sapphire, where the mismatch is ~16%. Their approach is referred to as two-step epitaxy. The process entails the growth of GaN at low temperature, fol-

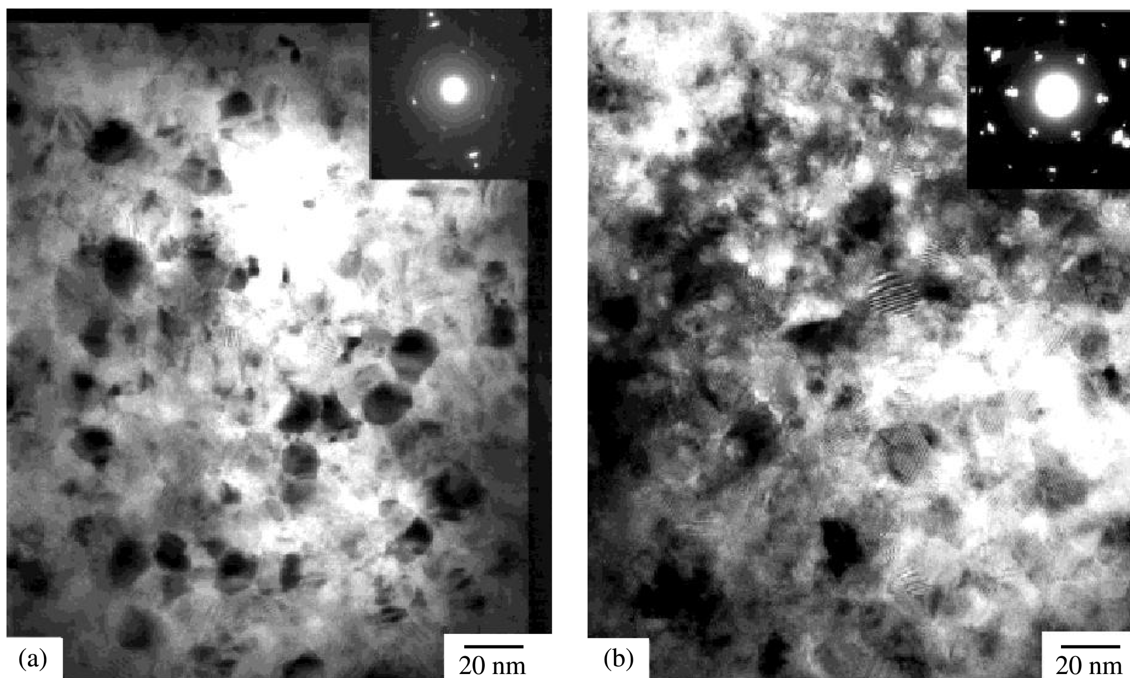


Fig. 14. Plan-view (0001) BF images of (a) as-grown and (b) annealed GaN NLs.

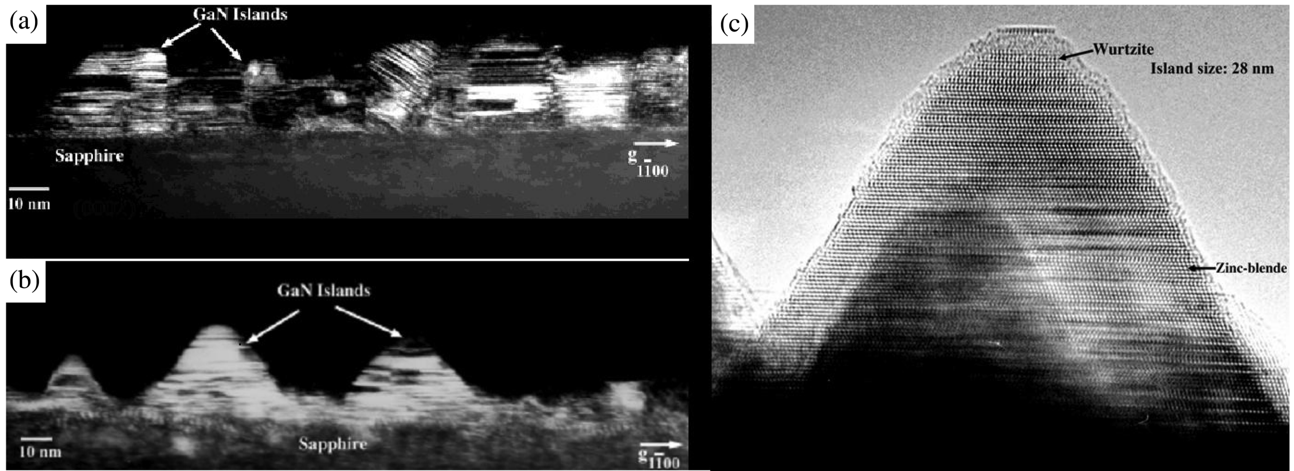


Fig. 15. WB images of (a) as-grown and (b) annealed GaN NLs. The NLs were deposited for 3 min at 530 °C and 300 mbar and annealed to 1030 °C. (c) HRTEM image of an island in the annealed GaN NL.

lowed by a ramp up to high temperature for additional growth. Akasaki *et al.*[36] were able to obtain continuous films using this approach.

To understand two-step epitaxy, Lorenz *et al.*[38] and Narayanan *et al.*[39] investigated in detail the growth of GaN on (0001) sapphire by metalorganic chemical vapor deposition. They showed for the first time that the layers deposited at low temperature are single crystals, but contain subgrains; the in-plane misorientation between the subgrains is ~5, see Fig. 14. In cross-section, the layers appear to be highly defective and exhibit some tilted islands, Fig. 15(a). After annealing that occurred during ramp up, the layers evolved into three-dimensional islands, Fig. 15(b). During additional growth at high temperature, these islands grew laterally and coalesced. They did not observe dislocations at the coalescence front as was hypothesized previously by Wu *et al.*[40], see Fig. 16. The studies of Lorenz *et al.*[38] and Narayanan *et al.*[39] indicated that a major portion of threading dislocations evolve from highly defective low temperature layers as shown in Fig. 17, resulting in a density of 10^{10} cm^{-2} in fully grown layers.

As indicated earlier, defects have deleterious effects on the performance and reliability of minority carrier devices[8]. So, we must reduce the density of dislocations in integrated structures. A number of approaches are available to achieve this objective: lateral epitaxial overgrowth (ELOG) and its variants[26], nanoepitaxy[27, 28] and diffusion bonding [29-31].

ELOG has its merits and demerits. Its biggest demerit is that the density of threading dislocations is not uniform across the layer. There are regions of high and low dislocation densities. ELOG involves seeded growth of layers, followed by their lateral growth over dielectric masks used in this approach. Regions which are over the mask have low dislocation densities. However, when the lateral growth fronts coalesce, high dislocation densities develop in the coalescence regions. This occurs because independently seeded growths acquire tilts as they propagate across the mask. This variation in dislocation densities across the layer could affect yield and performance of devices fabricated from such layers.

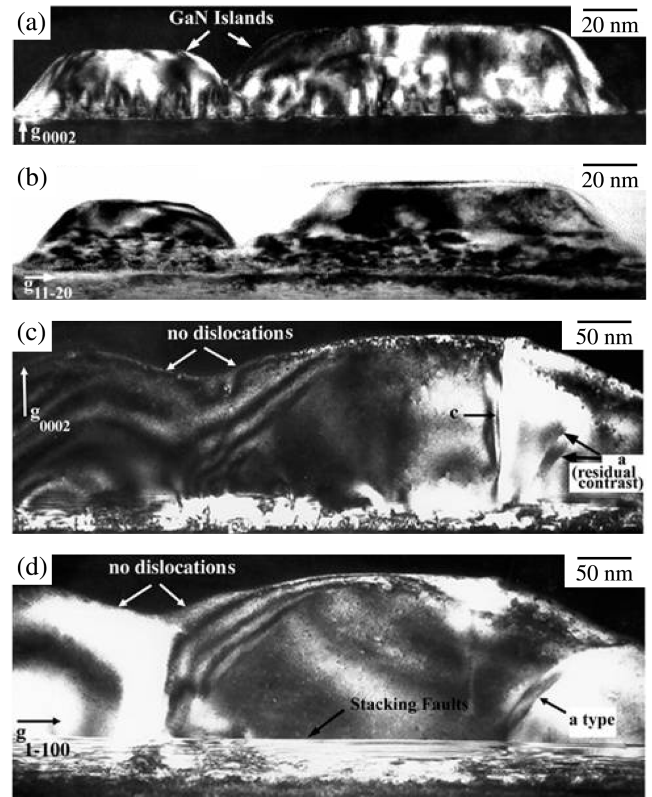


Fig. 16. (a), (b) WB and BF cross-sectional images of GaN islands after HT GaN growth for 20s obtained using (a) the (0002) and (b) the (11$\bar{2}$0) reflections. (c), (d) WB cross-sectional images after HT GaN growth for 75s obtained using (c) the (0002) and (d) the (1$\bar{1}$00) reflections.

We may be able to obviate the above problems using

Fig. 17. Weak beam cross-sectional image of a fully grown GaN epitaxial layer obtained using the $(11\bar{2}0)$ reflection.

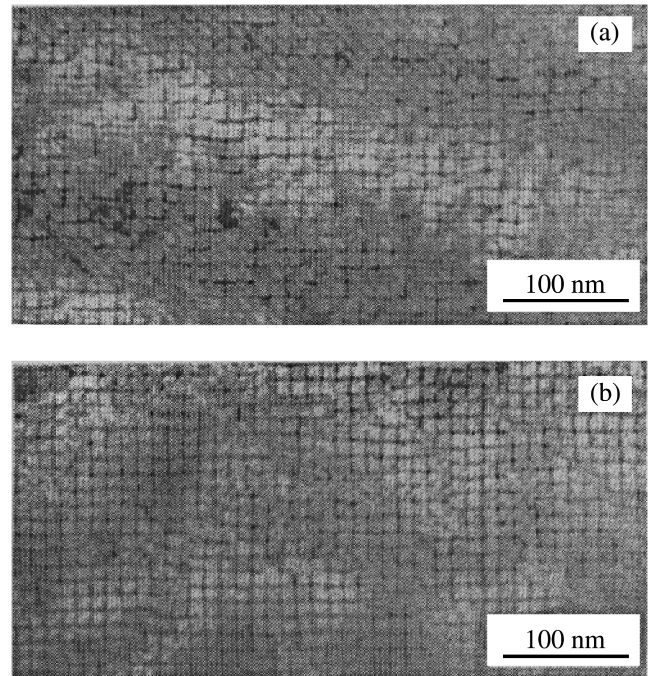


Fig. 19. (a) Plan-view TEM of the GaAs/InP interface showing the misfit dislocation network. It clearly shows that covalent bonds form even at low temperatures. (b) Plan-view TEM of the GaAs/InP interface after heat treatment at 650 °C for 30 min. The misfit dislocation network exhibits a more regular structure, including reactions with 60 ° locations, indicating that the interface is relaxed.

nanoepitaxy[27, 28]. At Arizona State University, we are applying this approach to grow GaN layers with low dislocation densities on (0001) sapphire. We show in Fig. 18 a hexagonal feature, fabricated into sapphire using focused ion beam[32]. The hexagonal feature is separated from the substrate by a trench. Two distinct situations could arise during the growth of GaN on the hexagonal feature. The growth is canted either outwards or inwards. The free surfaces associated with either of the two growth shapes would provide surfaces for the termination of dislocations. Subsequently, we plan to tailor growth conditions so as to enhance lateral growths from many such hexagons, resulting in a continuous layer. Since a dielectric mask is not involved and since in principle we can reduce separation between hexagons to small values, we could grow layers with low dislocation densities that would be randomly distributed. We refer to our approach as “Patterned Cantilever Epitaxy.”

Diffusion bonding between two dissimilar materials can be accomplished with or without an intervening layer which could be amorphous. In the absence of an intervening layer, misfit dislocations are observed at the interface between the two materials being bonded[30, 31]. These misfit dislocations can be considered to be geometrically necessary. Figure 19 taken from the study of Akatsu *et al.*[31] on diffusion-bonded GaAs/InP interfaces clearly show the misfit dislocation network. The network forms during bonding at low temperatures, Fig. 19(a), and is stable at high temperature, Fig. 19(b). This network is confined to the interface and does not have threading dislocations associated with it.

An interesting question concerns the bonding of wafers having large areas: does the bonding have to start in one area and then propagate outwards to complete the process? Figure 20 shows schematically a situation that may develop when bonding is initiated at two different regions, referred to as islands I and II in Fig. 20(a). If misfit dislocations AB and CD are aligned with each other, the two islands will coalesce forming one misfit dislocation AD, Fig. 20(b). However, if AB and CD are not aligned with each other, threading dislocations BC and EF must form, Fig. 20(c), because dislocations cannot terminate within a crystal. This implies that the fabrication of high quality structures from dissimilar materials using diffusion bonding will require careful processing.

4.2. Growth of Low Dimensional Structures

We know that electrons in a solid have discrete energy levels. We can effect changes in these levels by confining them in one-, two- and three-dimensions. We can accomplish this objective by fabricating low dimensional structures consisting of quantum wells, quantum wires and quantum-dots.

Using growth on patterned substrates, we can fabricate quantum wells and wires[33]. Let us imagine a situation in which we sequentially deposit two materials, differing in

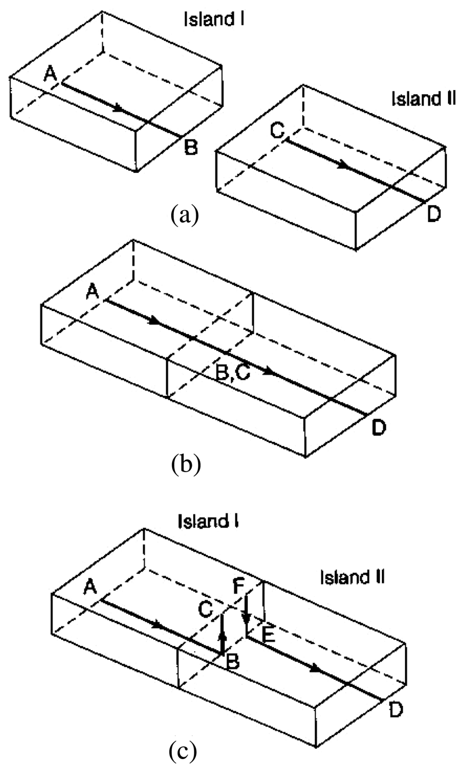


Fig. 20. Schematics illustrating the formation of threading dislocations BC and EF after the coalescence of islands I and II: (a) initial stage, (b) after coalescence when misfit dislocations AB and CD are aligned and (c) after coalescence when the misfit dislocations are not aligned. Note that the threading dislocations BC and EF have the same Burgers vector, but are opposite in sense. For the sake of clarity, substrate is not shown.

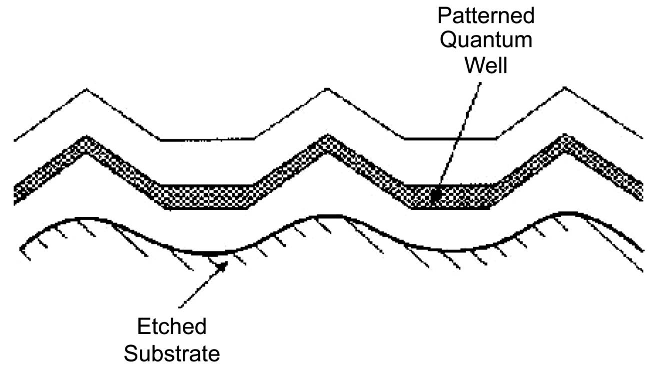


Fig. 21. Schematic cross-sectional view of a patterned quantum-well heterostructure formed after growth on a nonplanar substrate[33].

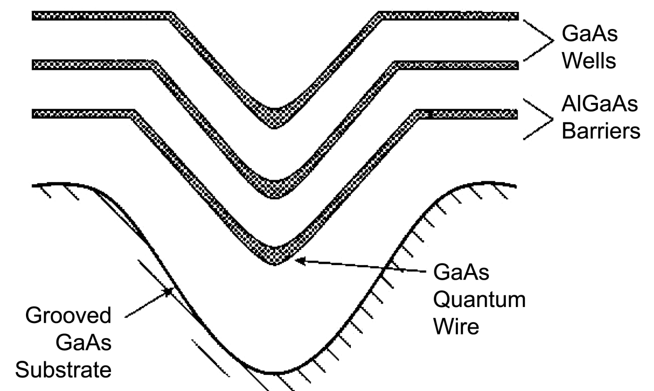


Fig. 22. Schematic cross section of a GaAs-GaAlAs heterostructure, grown by OMVPE in a $[01\bar{1}]$ groove in a (100) GaAs substrate, showing the formation of a crescent-shape quantum wire[33].

their band gaps, on a nonplanar substrate. The resulting quantum wells are shown in Fig. 21. The carriers can move in the plane of the quantum well, but not along the normal direction because of barriers.

The lateral patterning of the layers in Fig. 21 occurs because of the crystal facets exposed on a patterned substrates have different growth rates. The difference in the incorporation rate of atoms and lateral variation in flux of the growth species due to geometrical and/or surface diffusion effects cause the variation in growth rate.

Quantum wires having lateral dimensions in the 10 nm range can also be fabricated by exitaxial growth on patterned substrates. The schematic in Fig. 22 shows the GaAs/GaAlAs quantum-wire heterostructure grown by metalorganic chemical vapor depositions on a [011] oriented channel etched in a (100) GaAs substrate[33]. The growth of GaAlAs layers sharpens the corner between the exposed $\{111\}_{III}$ planes of the grooved substrate. Subsequent growth of a thin GaAs quantum-well layer increases the corner radius slightly because the migration distance of gallium is greater than that of aluminum, resulting in a crescent shape GaAs quantum wire. We can regain the sharpness of the corner by growing a thick GaAlAs barrier layer as shown in Fig. 22. Using sequential growths of GaAs and GaAlAs, we can obtain multiple quantum wells and quantum wires within a single groove. Figure 23 shows a cross-sectional electron micrograph of such an array, taken from the study of Kapon[33].

That quantum wells and quantum wires in Fig. 23 have different effective band gaps can be discerned from Fig. 24 that shows a cathodoluminscence (CL) spectrum from an array[34]. The CL emissions from the quantum wires (QWRS) and quantum wells (QWLS) occur at 770 and 660 nm, respectively, whereas the underlying GaAs substrate emits at 820 nm.

Recently, isolated and forests of quantum wires were synthesized using the concept of vapor-liquid-solid (VLS) growth, developed at the Bell Telephone Laboratories in the early sixties. Lars Samuelson of the University of Lund carried out pioneering studies on the growth of III-V quantum wires and heterojunctions. This approach has considerable potential because it permits accessibility to individual wires for the fabrication devices and structures.

The fabrication of quantum dots (QDs) that are uniformly distributed and have uniform distribution across a wafer sur-

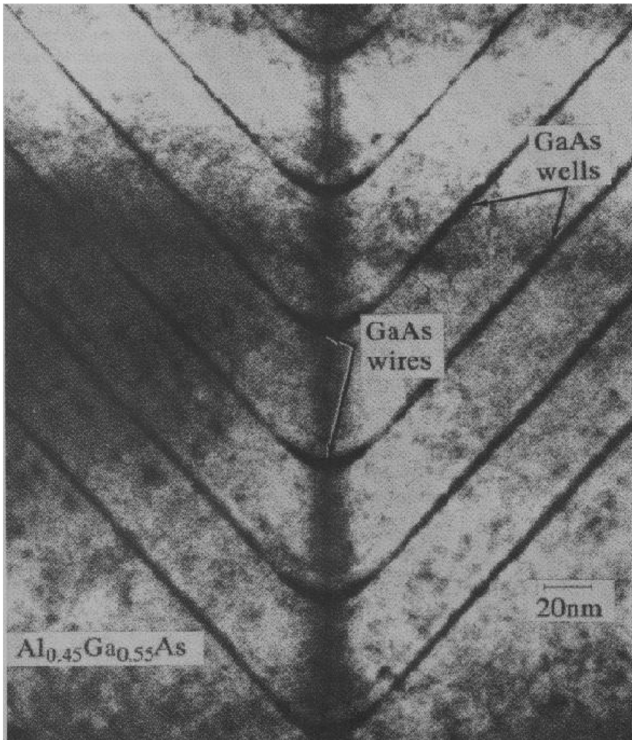


Fig. 23. Cross-sectional electron micrograph showing a vertical array of GaAs-GaAlAs quantum wires formed in a groove[33].

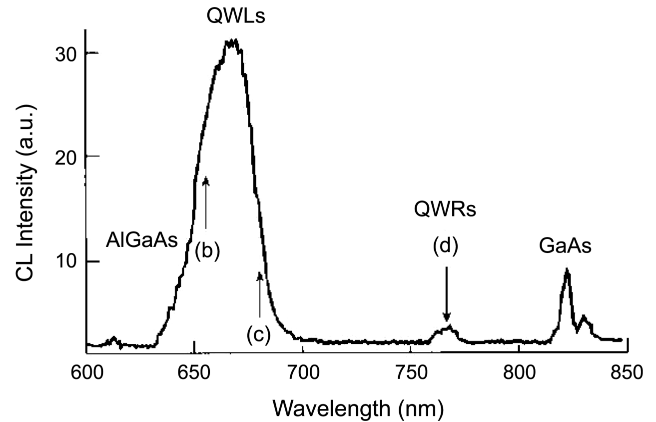


Fig. 24. Cathodoluminescence spectrum[34].

face is one of the most challenging, unresolved problems in materials science and engineering. This stems from the fact that self-assembly of QDs, an approach commonly used to synthesize them, leads to non-uniformity in sizes as well as distribution. These features are due to the statistical nature of the self-assembly process. Therefore, to accomplish the desired objective, we need to bias the assembly of atoms. Various approaches have been attempted, but they lack simplicity. One promising approach appears to be the use of stress fields of buried dislocation networks to form QDs at specific sites[35]. It is also likely that in this case QDs may from simultaneously, leading to uniformity in size.

5. SUMMARY

We have attempted to demonstrate that materials science played a crucial role in the evolution of microelectronics in the past, has a significant role in the present, and will have even a more important role in the future as the density of components on a chip increase substantially. This is so because we do not yet fully understand the behavior of materials at extremely small length scales.

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